

# SUPER<sup>®</sup>

SUPER 370SBA  
SUPER 370SBM  
SUPER 370SLA  
SUPER 370SLM

## USER'S AND BIOS MANUAL

Revision 1.1

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## Preface

### About This Manual

This manual is written for system houses, PC technicians and knowledgeable PC end users. It provides information for the installation and use of the SUPER 370SBA/370SBM/370SLA/370SLM motherboard. SUPER 370SBA/370SBM/370SLA/370SLM motherboards support Intel® Celeron™ 333/366 MHz or higher PPGA processors.

The addition of the Intel Celeron processor family with the Dual Independent Bus Architecture is housed in a package called the Plastic Pin Grid Array (PPGA). This package and its associated "370-pin socket" infrastructure will provide the headroom for future low-cost, high-performance processors.

### Manual Organization

Chapter 1, Introduction, describes the features, specifications and performance of the SUPER 370SBA/370SBM/370SLA/370SLM system board, provides detailed information about the chip set and offers warranty information.

Refer to Chapter 2, Installation, for instructions on how to install the Celeron PPGA processor and the heat sink support. This chapter provides you with instructions for handling static-sensitive devices. Read this chapter when you want to install DIMMs and to mount the system board in the chassis. Also refer to this chapter to connect the floppy and hard disk drives, IDE interfaces, the parallel port and the serial ports, as well as the cables for the power supply, the reset button, the Keylock/Power LED, the speaker and the keyboard.

If you encounter any problems, please see Chapter 3, Troubleshooting, which describes troubleshooting procedures for the video, memory and the setup configuration stored in memory. For quick reference, a general FAQ (Frequently Asked Questions) section is provided. Instructions are also included for technical support procedures, for returning merchandise for service and for BIOS upgrades using our BBS#.

See Chapter 4 for configuration data and BIOS features.

Chapter 5 has information on running setup and includes default settings for Standard Setup, Advanced Setup, Chipset function, Power Management, PCI/PnP Setup, and Peripheral Setup.

Appendix A offers information on BIOS error beep codes and messages.

Appendix B shows post diagnostic error messages.

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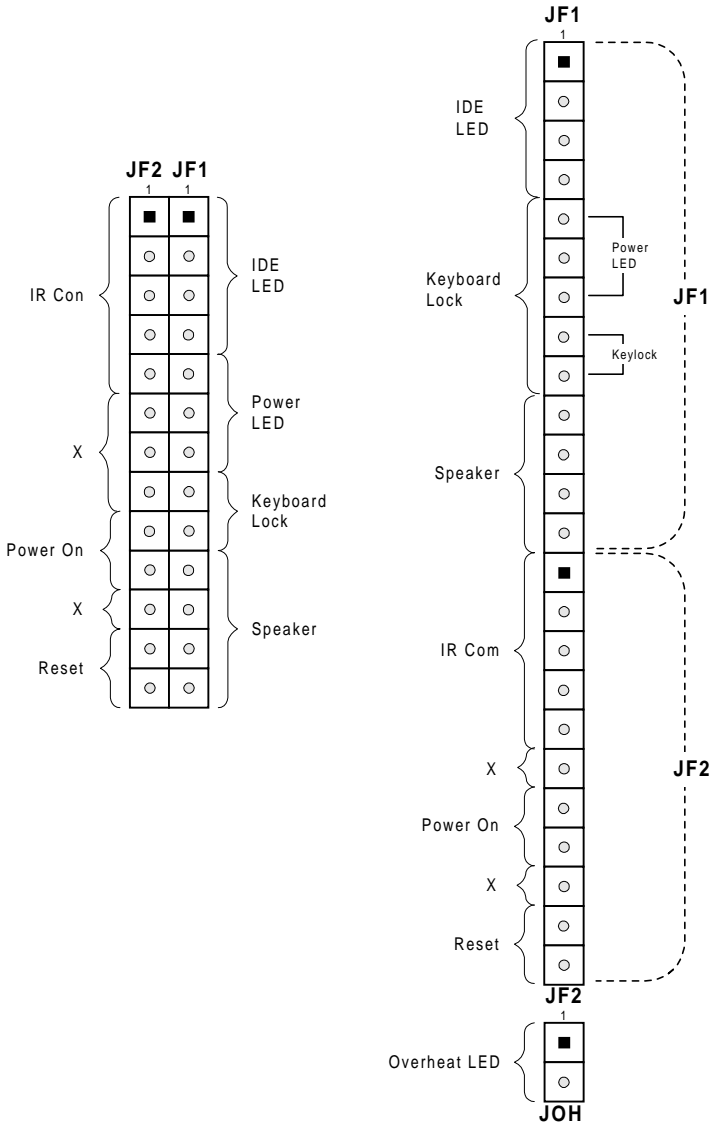
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## Jumpers Quick Reference

370SBM	370SBA/ 370SLA/ 370SLM		
Jumpers	Jumpers	Function	Page
JBT1	JBT1	CMOS Clear	2-6
JPWAKE	JPWAKE	Keyboard Wake-Up	2-7
JP11	JP11	Bus Speed	2-7
Connectors	Connectors	Function	Page
J8	J8	AGP Port	2-11
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JF1: 8-9	JF1: 8-9	Keylock	2-5
JF1: 10-13	JF1: 10-13	Speaker	2-5
JF2: 1-5	JF2: 1-5	IR (Infrared) Connector	2-4
JF2: 9-10	JF2: 7-8	Power ON Switch	2-4
JF2: 12-13	JF2: 10-11	Reset Switch	2-4
JOH: 1-2	JOH: 1-2	Overheat LED	2-7
JL1	JL1	Chassis Intrusion Switch	2-7
JT1	JT1	CPU Fan	2-6
JT2	JT2	Chassis Fan	2-6
JT3	JT3	Thermal Control Fan	2-6
WOL	WOL	Wake-on-LAN	2-6



## Front Control Panel Connector



Please see pages 2-4 through 2-7 for pin definitions.

## Notes

# Chapter 1

## Introduction

### 1-1 Overview

The SUPER 370SBA/370SBM/370SLA/370SLM motherboards support single Intel® Celeron™ 333/366 MHz or higher Plastic Pin Grid Array (PPGA) processors at a 66 MHz front side bus speed. (The 100 MHz FSB speed is only available when using 100 MHz FSB Celeron processors.) The SUPER 370SBA and 370SBM motherboards are based on Intel's 440BX chip set, and the SUPER 370SLA and 370SLM motherboards are based on Intel's 440LX chip set. Both 440BX and 440LX chip sets enable an Accelerated Graphics Port (AGP), Wake-on-LAN™, synchronous DRAM (SDRAM), concurrent PCI and dual IDE channels that support Ultra DMA 33 MB/s burst data transfer rate.

The SUPER 370SBA and 370SLA are ATX form factor motherboards and have 4 PCI and 3 ISA slots. The SUPER 370SBM and 370SLM are microATX form factor motherboards and have 3 PCI and 1 ISA slots. All four motherboards have an AGP port, and can accommodate a total of 384 MB PC100 unbuffered SDRAM memory with three 168-pin dual inline memory module (DIMM) sockets. The SUPER 370SBA and 370SBM motherboards can support the 100 MHz front side bus speed for future Celeron PPGA upgrades, and its 440BX chip set allows you to install up to 768 MB of PC100 registered SDRAM. The SUPER 370SLA and 370SLM motherboards support the 66 MHz system bus speed only, and can accept either PC66 EDO or PC100 SDRAM DIMMs.

AGP reduces contention between the CPU and I/O devices by broadening the graphics bandwidth to memory. It delivers a maximum of 532 MB/s in the 2x transfer mode, which is quadruple the PCI speed!

Wake-On-LAN (WOL) allows for remote network management and configuration of the PC, even in off-hours when the PC is turned off. This reduces the complexity of managing the network.

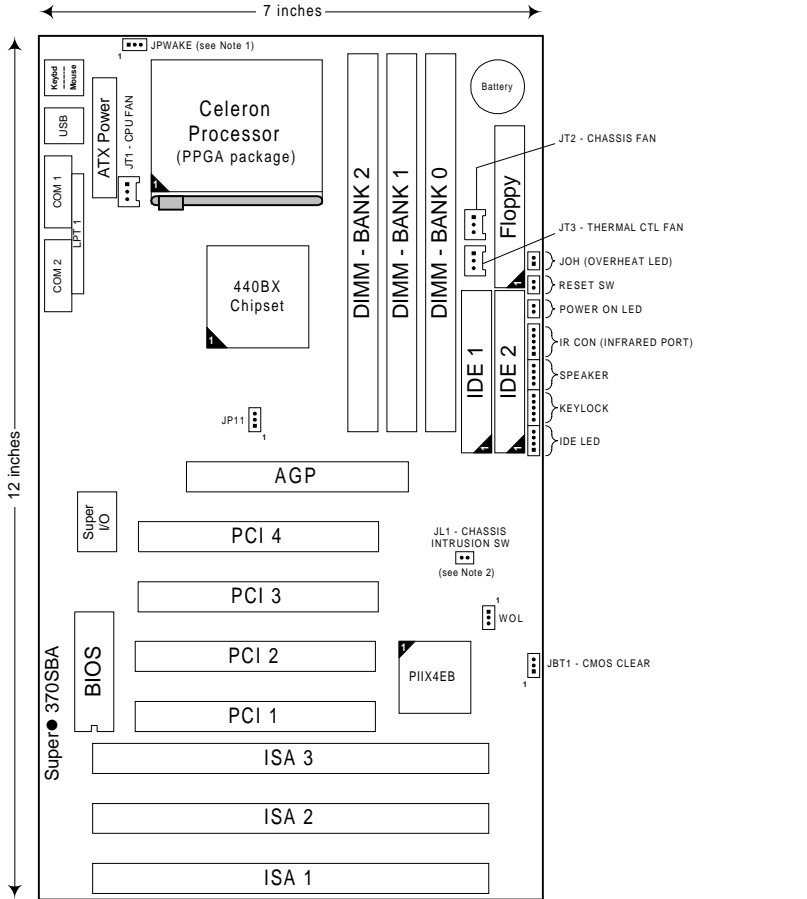
Other features that maximize customer satisfaction and simplicity in managing the computer are its support for the PC 98 and the Advanced Configuration and Power Interface (ACPI) standards. With PC Health Monitoring, you can protect your system from problems before they even occur.

All motherboards include the following I/O: 2 IDE ports, a floppy port, an ECP/EPP supported parallel port, PS/2 mouse and PS/2 keyboard ports, 2 serial ports, an infrared port and 2 USB ports.

## SUPER 370SBA

Figure 1-1. SUPER 370SBA Motherboard Image





Jumper Settings

- JPWAKE:** 1-2 Disable Keyboard Wake-Up (default)  
 2-3 Enable Keyboard Wake-Up (see Note 1)
- JP11:** 1-2 Auto Select Bus Speed  
 2-3 66MHz Bus Speed  
 OFF 100MHz Bus Speed
- JBT1:** 1-2 Normal  
 2-3 CMOS Clear

Notes

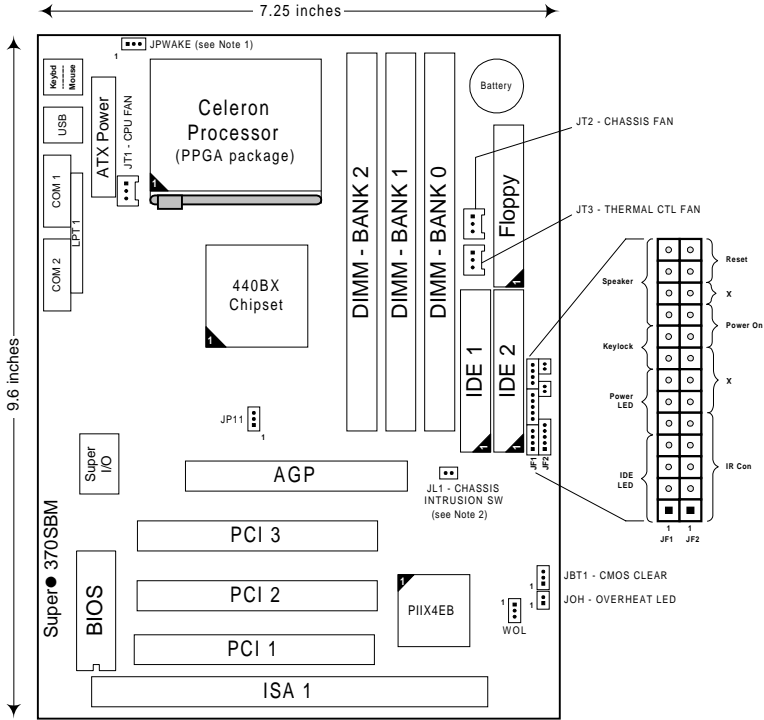
- 1 To enable Keyboard Wake-Up, set JPWAKE jumper to 2-3 and ENABLE Keyboard Wake-Up function in system BIOS.
- 2 Chassis Intrusion Switch (JL1) is normally open. If connected to chassis switch, removing chassis cover causes switch input to close.
- 3 No CPU jumper settings are required for the Celeron (333/366 MHz) processor. The settings are preset (fixed bus ratio) in the processor.

**Figure 1-2. SUPER 370SBA Motherboard Layout**

## SUPER 370SBM

Figure 1-3. SUPER 370SBM Motherboard Image





Jumper Settings

- JPWAKE: 1-2 Disable Keyboard Wake-Up (default)  
 2-3 Enable Keyboard Wake-Up (see Note 1)
- JP11: 1-2 Auto Select Bus Speed  
 2-3 66MHz Bus Speed  
 OFF 100MHz Bus Speed
- JBT1: 1-2 Normal  
 2-3 CMOS Clear

Notes

- 1 To enable Keyboard Wake-Up, set JPWAKE jumper to 2-3 and ENABLE Keyboard Wake-Up function in system BIOS.
- 2 Chassis Intrusion Switch (JL1) is normally open. If connected to chassis switch, removing chassis cover causes switch input to close.
- 3 No CPU jumper settings are required for the Celeron (333/366 MHz) processor. The settings are preset (fixed bus ratio) in the processor.

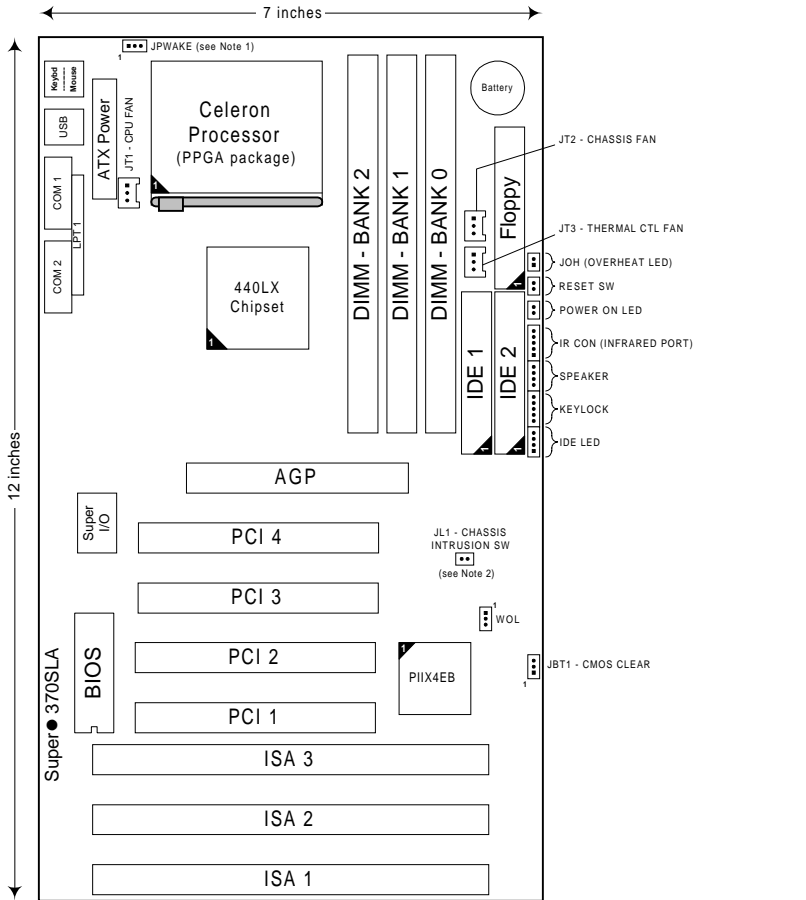
Figure 1-4. SUPER 370SBM Motherboard Layout

## SUPER 370SLA

Figure 1-5. SUPER 370SLA Motherboard Image







## Jumper Settings

- JPWAKE: 1-2 Disable Keyboard Wake-Up (default)  
2-3 Enable Keyboard Wake-Up (see Note 1)
- JBT1: 1-2 Normal  
2-3 CMOS Clear

## Notes

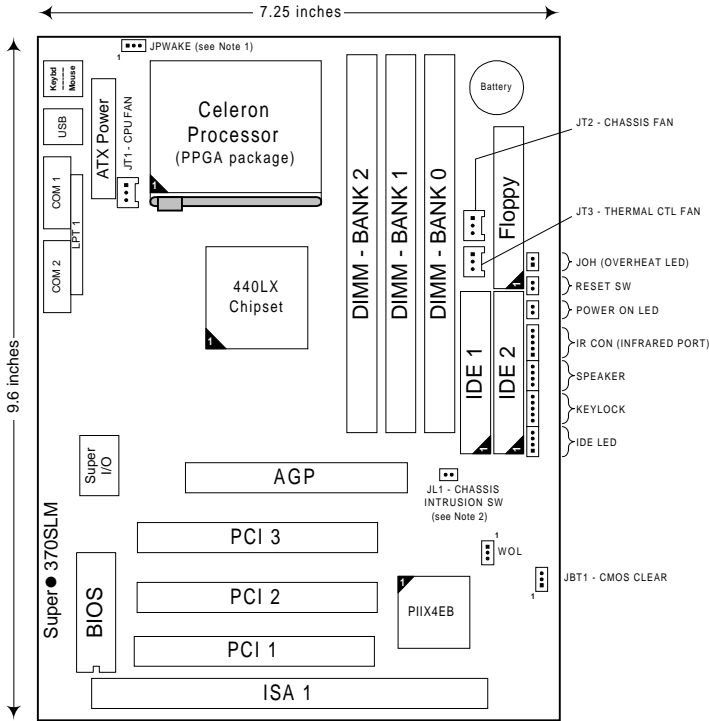
- 1 To enable Keyboard Wake-Up, set JPWAKE jumper to 2-3 **and** ENABLE Keyboard Wake-Up function in system BIOS.
- 2 Chassis Intrusion Switch (JL1) is normally open. If connected to chassis switch, removing chassis cover causes switch input to close.
- 3 No CPU jumper settings are required for the Celeron (333/366 MHz) processor. The settings are preset (fixed bus ratio) in the processor.

Figure 1-6. SUPER 370SLA Motherboard Layout

## SUPER 370SLM

Figure 1-7. SUPER 370SLM Motherboard Image





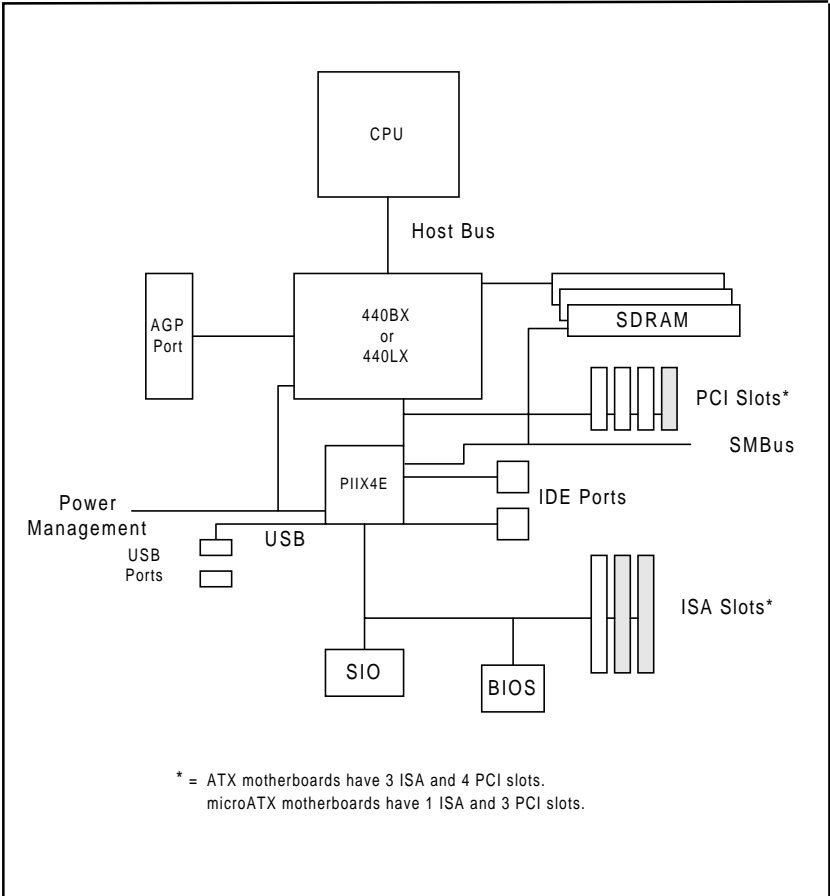
— Jumper Settings —

- JPWAKE: 1-2 Disable Keyboard Wake-Up (default)  
 2-3 Enable Keyboard Wake-Up (see Note 1)
- JBT1: 1-2 Normal  
 2-3 CMOS Clear

— Notes —

- 1 To enable Keyboard Wake-Up, set JPWAKE jumper to 2-3 **and** ENABLE Keyboard Wake-Up function in system BIOS.
- 2 Chassis Intrusion Switch (JLI) is normally open. If connected to chassis switch, removing chassis cover causes switch input to close.
- 3 No CPU jumper settings are required for the Celeron (333/366 MHz) processor. The settings are preset (fixed bus ratio) in the processor.

**Figure 1-8. SUPER 370SLM Motherboard Layout**



**Figure 1-9. 440BX/LX AGP Chip Set:  
System Block Diagram**

## 1-2 Features of the 370SBA, 370SBM, 370SLA and 370SLM Motherboards\*

\* **Bold text indicates variations in features.**

The following list covers the general features of the 370SBA, 370SBM, 370SLA and 370SLM motherboards.

### CPU

- Single Celeron 333/366/400 MHz PPGA processors at a 66 MHz front side bus speed. (The 100 MHz FSB speed is only available when using 100 MHz FSB Celeron processors. For future processor support, check our web site at <http://www.supermicro.com>.)

### Memory

- 384 MB EDO or 384 MB unbuffered 3.3V SDRAM at 66 MHz (**370SLA and 370SLM only**)
  - 384 MB EDO or 384 MB unbuffered 3.3V SDRAM, or 768 MB registered SDRAM (**370SBA and 370SBM only**)
- (Note: The maximum cacheable memory size depends on the processor capabilities.)
- Error Checking and Correction and Error Checking support

### Chip Set

- Intel 440BX for 370SBA and 370SBM
- Intel 440LX for 370SLA and 370SLM

<u>Expansion Slots</u>	
370SBA / 370SLA	370SBM / 370SLM
<ul style="list-style-type: none"> <li>• 4 PCI slots</li> <li>• 3 ISA slots</li> </ul> [one shared PCI/ISA slot]	<ul style="list-style-type: none"> <li>• 3 PCI slots</li> <li>• 1 ISA slots</li> </ul> [one shared PCI/ISA slot]
• 1 AGP slot	• 1 AGP slot

### BIOS

- 2 Mb AMI® Flash BIOS
- APM 1.2, DMI 2.1, Plug and Play (PnP)
- ACPI Support

### PC Health Monitoring

- Seven onboard voltage monitors for CPU core(s), CPU I/O, +3.3V, ±5V, and ±12V
- Three-fan status monitors with firmware/software on/off control
- Environmental temperature monitor and control
- CPU fan auto-off in sleep mode
- Chassis overheat LED and thermal fan control

- Chassis intrusion detection
- System resource alert
- Hardware BIOS virus protection
- Switching voltage regulator for the CPU core
- SUPERMICRO SUPER Doctor and Intel® LANDesk® Client Manager (LDCM) support (optional)

#### ACPI/PC 98 Features

- Microsoft OnNow
- Slow blinking LED for suspend state indicator
- BIOS support for USB keyboard
- Real-time clock wake-up alarm
- Main switch override mechanism
- External modem ring-on

#### On-Board I/O

- 2 EIDE Bus Master interfaces support Ultra DMA/33 and Mode 4
- 1 floppy port interface
- 2 Fast UART 16550 serial ports
- 1 parallel port that supports EPP (Enhanced Parallel Port) and ECP (Extended Capabilities Port)
- PS/2 mouse and PS/2 keyboard
- Infrared port
- 2 USB (Universal Serial Bus) ports

#### CD Utilities

- Intel LANDesk Client Manager for Windows NT® and Windows® 95 (optional)
- PIIX4 Upgrade Utility for Windows 95
- BIOS Flash Upgrade Utility
- SUPER Doctor Utility

#### Dimensions

- SUPER 370SBA - ATX (12" x 7")
- SUPER 370SBM - microATX (9.6" x 7.25")
- SUPER 370SLA - ATX (12" x 7")
- SUPER 370SLM - microATX (9.6" x 7.25")

## 1-3 Chip Set Overview

### 440BX Chip Set

The 440BX chip set, developed by Intel, is the ultimate processor platform targeted for 3D graphics and multimedia applications. Along with a System-to-PCI bridge integrated with an optimized DRAM controller and data path, this chip set supports the Accelerated Graphics Port (AGP) interface. AGP is a high performance, component level interconnect targeted at 3D applications and based on a set of performance enhancements to PCI. The I/O subsystem portion of the 440BX platform is based on the PIIX4E, a highly integrated version of Intel's PCI-to-ISA bridge family.

The PCI/AGP and system bus interface controller (82443BX) supports one Celeron processor. It provides an optimized 72-bit DRAM interface (64 bits of data plus ECC) that supports 3.3V DRAM technology. The controller provides the interface to a PCI bus operating at 33 MHz. This interface implementation is compliant with the PCI Rev 2.1 Specification. The AGP interface is based on AGP Specification Rev 1.0. It can support data transfer rates of up to 133 MHz (532 MB/s).

### 440LX Chip Set

The 440LX chip set, developed by Intel, is a high-performance processor platform targeted for existing 3D graphics and multimedia applications. Along with a System-to-PCI bridge integrated with an optimized DRAM controller and data path, this chip set supports the Accelerated Graphics Port (AGP) interface. AGP is a high performance, component level interconnect targeted at 3D applications and based on a set of performance enhancements to PCI. The I/O subsystem portion of the 440LX platform is based on the PIIX4, a highly integrated version of Intel's PCI-to-ISA bridge family.

The 440LX PCI/AGP Controller (PAC) system bus interface supports one Celeron processor. It provides an optimized 72-bit DRAM interface (64 bits of data plus ECC) that supports 3.3V DRAM technology. The PAC provides the interface to a PCI bus operating at 33 MHz. This interface implementation is compliant with the PCI Rev 2.1 Specification. The AGP interface is based on AGP Specification Rev 1.0. It can support data transfer rates of up to 133 MHz (532 MB/s).

## 1-4 PC Health Monitoring

This section describes the PC health monitoring features of the SUPER 370SBA, 370SBM, 370SLA and 370SLM. All have an onboard System Hardware Monitor chip that supports PC health monitoring.

### **Seven Onboard Voltage Monitors for the CPU Core(s), CPU I/O, +3.3V, $\pm 5V$ , and $\pm 12V$**

The onboard voltage monitor scans these seven monitored voltages continuously. Once a voltage becomes unstable, it will give a warning or send an error message to the screen. Users can adjust the voltage thresholds to define the sensitivity of the voltage monitor.

**Note:** *-5V is not required when using a microATX (SFX) power supply.*

### **Three-Fan Status Monitors with Firmware/Software On/Off Control**

The PC health monitor can check the RPM status of the cooling fans. The onboard 3-pin CPU fan is controlled by the ACPI BIOS and the ACPI-enabled operating system. The thermal fans are controlled by the overheat detection logic.

### **Environmental Temperature Control**

The thermal control sensor monitors the CPU temperature in real-time and will turn on a back-up fan whenever the CPU temperature exceeds a user-defined threshold. The overheat circuitry runs independently from the CPU. It can continue to monitor for overheat conditions even when the CPU is in sleep mode. Once it detects that the CPU temperature is too high, it will automatically turn on the back-up fan to prevent any overheat damage to the CPU. The onboard chassis thermal circuitry can monitor the overall system temperature and alert users when the chassis temperature is too high.

### **CPU Fan Auto-Off in Sleep Mode**

The CPU fan activates when the power is turned on. It can be turned off when the CPU is in sleep mode. When in sleep mode, the CPU does not run at full power, and thereby generates less heat. For power saving purposes, the user has the option to shut down the CPU fan.



### **CPU Overheat LED and Thermal Fan Control**

This feature is available when the user enables the CPU overheat warning function in the BIOS (see page 5-17). The overheat sensor is triggered when the CPU temperature exceeds the temperature configured by the user. When the overheat sensor is triggered, both the overheat fan and the warning LED are activated.

### **Chassis Intrusion Detection**

The chassis intrusion circuitry can detect unauthorized intrusion to the system. The chassis intrusion connector is located on JL1. Attach a microswitch to JL1. When the microswitch is closed, it means that the chassis has been opened. The circuitry will then alert the user with a warning message when the system is turned on. This feature is available when the user is running Intel's LANDesk Client Manager and SUPERMICRO's Super Doctor.

### **System Resource Alert**

This feature is available when used with Intel's LANDesk Client Manager. It is used to notify the user of certain system events. For example, if the system is running low on virtual memory and there is insufficient hard drive space for saving the data, you can be alerted of the potential problem.

### **Hardware BIOS Virus Protection**

The system BIOS is protected by hardware so that no virus can infect the BIOS area. The user can only change the BIOS content through the flash utility provided by SUPERMICRO. This feature can prevent viruses from infecting the BIOS area and destroying valuable data.

### **Switching Voltage Regulator for the CPU Core**

The switching voltage regulator for the CPU core can support up to 20A of current, with the auto-sensing voltage ID ranging from 1.8V to 3.5V. This will allow the regulator to run cooler and thus make the system more stable.

## **Intel LANDesk® Client Manager (LDCM) Support**

As the computer industry grows, PC systems have become more complex and harder to manage. Historically, only experts have been able to fully understand and control these complex systems. Today's users want manageable systems that they can interact with automatically. Client Manager enables both administrators and clients to:

- Review system inventory
- View DMI-compliant component information
- Back up and restore system configuration files
- Troubleshoot
- Receive notifications of system events
- Transfer files to and from client workstations
- Remotely boot up client workstations

## **1-6 ACPI/PC 98 Features**

ACPI stands for Advanced Configuration and Power Interface. The ACPI specification defines a flexible and abstract hardware interface that provides a standard way to integrate power management features throughout a PC system, including its hardware, operating system and application software. This enables the system to automatically turn on and off peripherals such as CD-ROMs, network cards, hard disk drives and printers. This also includes consumer devices connected to the PC such as VCRs, TVs, telephones and stereos.

In addition to enabling operating system-directed power management, ACPI provides a generic system event mechanism for Plug and Play and an operating system-independent interface for configuration control. ACPI leverages the Plug and Play BIOS data structures while providing a processor architecture-independent implementation that is compatible with both Windows 98 and Windows NT 5.0.

### **Microsoft OnNow**

The OnNow design initiative is a comprehensive, system-wide approach to system and device power control. OnNow is a term for a PC that is always on but appears off and responds immediately to user or other requests.

### **Slow Blinking LED for Suspend State Indicator**

When the CPU goes into a suspend state, the power LED will start blinking to indicate that the CPU is in suspend mode. When the user presses any key, the CPU will wake-up and the LED will automatically stop blinking and remain on.

### **BIOS Support for USB Keyboard**

If the USB keyboard is the only keyboard in the system, the USB keyboard will work like a normal keyboard during system boot-up.

### **Real-Time Clock Wake-up Alarm**

Although the PC may be perceived to be off when not in use, it is still capable of responding to preset wake-up events. In the BIOS, the user can set a timer to wake-up the system at a predetermined time (see page 5-14).

### **Main Switch Override Mechanism**

When an ATX power supply is used, the power button can function as a system suspend button. When the user depresses the power button, the system will enter a SoftOff state. The monitor will be suspended, and the hard drive will spin down. Depressing the power button again will cause the whole system to wake-up. During the SoftOff state, the ATX power supply provides power to keep the required circuitry in the system alive. In case the system malfunctions and you want to turn off the power, just depress and hold the power button for 4 seconds. The power will turn off and no power will be provided to the motherboard.

### **External Modem Ring-on**

Wake-up events can be triggered by a device such as the external modem ringing when the system is in SoftOff state. Note that external modem ring-on can only be used with an ATX 2.01 (or above) compliant power supply.

### **Wake-On-LAN (WOL)**

Wake-on-LAN is defined as the ability of a management application to remotely power up a computer that is powered off. Remote PC setup, updates and asset tracking can occur after hours and on weekends so daily LAN traffic is kept to a minimum and users are not interrupted.

The motherboards have a 3-pin header (WOL) used to connect to the 3-pin header on a Network Interface Card (NIC) that has WOL capability. Note that Wake-On-Lan can only be used with an ATX 2.01 (or above) compliant power supply.

## 1-7 Power Supply Requirements

As with all computer products, a stable power source is necessary for proper and reliable operation. It is even more important for processors that have high CPU clock rates of 300 MHz and above.

The SUPER 370SBA/370SBM/370SLA/370SLM accommodates ATX power supplies, and the 370SBM and 370SLM accommodates the new SFX power supplies. Although most power supplies generally meet the specifications required by the CPU, some power supplies are inadequate.

It is highly recommended that you use a high quality power supply which meets ATX Power Supply Specification 2.01. Additionally, in areas where noisy power transmission is present, you may choose to install a line filter to separate the computer from noise. It is recommended that you also install a power surge protector to help avoid problems caused by power surges.

## 1-8 Super I/O

The disk drive adapter functions of the Super I/O chip include a floppy disk drive controller that is compatible with industry standard 82077/765, a data separator, write pre-compensation circuitry, decode logic, data rate selection, a clock generator, drive interface control logic and interrupt and DMA logic. The wide range of functions integrated onto the Super I/O greatly reduces the number of components required for interfacing with floppy disk drives. The Super I/O supports four 360 K, 720 K, 1.2 M, 1.44 M or 2.88 M disk drives and data transfer rates of 250 Kb/s, 500 Kb/s or 1 Mb/s.

The Super I/O provides two high speed serial communication ports (16550 UARTs), one of which supports serial infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2 Kbps as well as an advanced speed with baud rates of 230 K, 460 K or 921 Kbps, which support higher speed modems.

The Super I/O supports one PC-compatible printer port (SPP), Bi-directional Printer Port (BPP), Enhanced Parallel Port (EPP) or Extended Capabilities Port (ECP). Extension FDD and Extension 2FDD Modes are also available through the printer port interface pins to allow one or two external floppy disk drives to be connected.

The Super I/O provides functions that comply with ACPI (Advanced Configuration and Power Interface), which includes support of legacy and ACPI power management through an SMI or SCI function pin. It also features auto power management to reduce power consumption.

The Super I/O complies with **Microsoft PC98 Hardware Design Guide**. IRQs, DMAs and I/O space resources can flexibly adjust to meet ISA PnP requirements. Moreover, it meets the specifications of PC98's power management requirements: ACPI and APM (Advanced Power Management).

**Notes**

## Chapter 2 Installation

### 2-1 Static-Sensitive Devices

Static-sensitive electrical discharge can damage electronic components. To prevent damage to your system board, it is important to handle it very carefully. The following measures are generally sufficient to protect your equipment from static discharge.

#### Precautions

- Use a grounded wrist strap designed to prevent static discharge.
- Touch a grounded metal object before you remove the board from the antistatic bag.
- Handle the board by its edges only; do not touch its components, peripheral chips, memory modules or gold contacts.
- When handling chips or modules, avoid touching their pins.
- Put the system board and peripherals back into their antistatic bags when not in use.
- For grounding purposes, be sure your computer system's chassis provides excellent conductivity between its power supply, the case, the mounting fasteners and the system board.

#### Unpacking

The system board is shipped in antistatic packaging to avoid static damage. When unpacking the board, be sure the person handling the board is static-protected.

## 2-2 Celeron PPGA Processor Installation

The Celeron PPGA processor resides in the 370-pin Zero Insertion Force (ZIF) socket on the motherboard.



### **CAUTION**

- 1. Always turn system power OFF before installing or removing any device.**
- 2. Always observe static electricity precautions when handling any components.**
- 3. Inserting the processor chip incorrectly may damage the chip.**
- 4. The processor requires the use of a heat sink/cooling device.**

Perform the following steps to install the Celeron PPGA processor:

1. Unlatch and lift the lever on the side of the 370-pin ZIF socket.

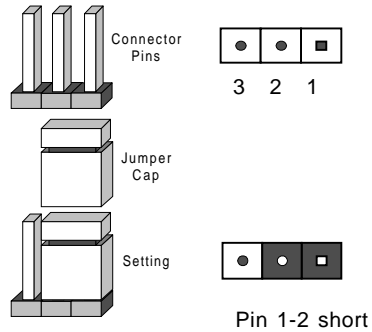


2. Carefully handle the processor chip by its edges and avoid touching any of the pins on the bottom of the chip.
3. The processor chip has a notch on one corner identifying pin 1. Pin 1 on the socket is located in the blank triangle area near the end of the lever (when latched). Align the notch (pin 1) on the chip with pin 1 on the socket, and carefully place the processor in the socket. The processor should slide easily into the socket.
4. Swing the lever to the down position and latch it to lock the processor in place.



## 2-3 Explanation and Diagram of Jumper/Connector

To modify the operation of the motherboard, jumpers can be used to choose between optional settings. Jumpers create shorts between two pins to change the function of the connector. Pin 1 is identified with a square.



## 2-4 Mounting the Motherboard in the Chassis

All the motherboards have standard mounting holes to fit different types of chassis. Chassis may come with a variety of mounting fasteners, made of metal or plastic. Although a chassis may have both metal and plastic fasteners, metal fasteners are the most highly recommended because they ground the system board to the chassis. Therefore, use as many metal fasteners as possible for better grounding.

## 2-5 Connecting Cables

### ATX Power Supply Connector

After you have securely mounted the motherboard to the chassis, you are ready to connect the cables. Attach a power supply cable to J32 for an ATX power supply. See Table 2-1 for the pin definitions of an ATX power supply.

**Table 2-1**  
ATX Power Supply Connector  
Pin Definitions for J32

Pin Number	Definition	Pin Number	Definition
1	3.3V	11	3.3V
2	3.3V	12	-12V
3	Ground	13	Ground
4	5V	14	PS-ON
5	Ground	15	Ground
6	5V	16	Ground
7	Ground	17	Ground
8	PW-OK	18	-5V
9	5VSB	19	5V
10	12V	20	5V

If installing a 370SBM or 370SLM microATX motherboard, an SFX power supply is recommended (though an ATX power supply also works with a microATX motherboard). Attach a power supply cable to J32 for an SFX power supply. See Table 2-2 for the pin definitions of an SFX power supply.

**Table 2-2**  
SFX Power Supply Connector  
Pin Definitions for J32

Pin Number	Definition	Pin Number	Definition
1	3.3V	11	3.3V/sense
2	3.3V	12	-12V
3	Ground	13	Ground
4	5V	14	PS-ON
5	Ground	15	Ground
6	5V	16	Ground
7	Ground	17	Ground
8	PW-OK	18	Reserved
9	5VSB	19	5V
10	12V	20	5V

Note: There is no -5V pin for SFX power.

## Infrared Connector

The infrared connector is located on pins 1-5 of JF2. See Table 2-3 for pin definitions.

**Table 2-3**  
Infrared Pin  
Definitions  
for JF2

Pin Number	Definition
1	+5V
2	Key
3	IRRX
4	Ground
5	IRTX

## PW\_ON Connector

The PW\_ON connector is located on pins 9 and 10 of JF2. Momentarily contacting both pins will power on/off the system. The user can also configure this button to function as a suspend button. (See BIOS setup information on page 5-12). To turn off the power when set to suspend mode, hold down the power button for at least 4 seconds. See Table 2-4 for pin definitions.

**Table 2-4**  
PW-ON Connector  
Pin Definitions  
for JF2

Pin Number	Definition
9	PW_ON
10	Ground

## Reset Connector

The reset connector is located on pins 12 and 13 of JF2. This connector attaches to the hardware reset switch on the computer case. See Table 2-5 for pin definitions.

**Table 2-5**  
Reset Pin  
Definitions  
for JF2

Pin Number	Definition
12	Ground
13	Reset

## Hard Drive LED Connector

The connector for the IDE hard drive LED is located on pins 1 to 4 of JF1. Attach the hard drive LED cable to pins 1 and 2. See Table 2-6 for pin definitions.

**Table 2-6**  
IDE Hard Drive LED  
Pin Definitions  
for JF1

Pin Number	Definition
1	+5V
2	HD Active
3	HD Active
4	+5V

## Keylock/Power LED Connector

The keylock/power LED connector is located on pins 5 to 9 of JF1. See Table 2-7 for pin definitions. Pins 5 and 7 are for the power LED. Pins 8 and 9 are for the keylock.

**Table 2-7**  
Keylock/Power LED Pin Definition for JF1

Pin Number	Function	Definition
5	VCC +5V	Red wire, LED power
6	VCC +5V	Red wire, LED power
7	Ground	LED control
8		Keyboard inhibit
9	Ground	Black wire

## Speaker Connector

The speaker connector is located on pins 10 to 13 of JF1. See Table 2-8 for pin definitions.

**Table 2-8**  
Speaker Connector Pin Definitions for JF1

Pin Number	Function	Definition
10	+	Red wire, Speaker data
11	Key	No connection
12		Key
13		Speaker data

## ATX PS/2 Keyboard and PS/2 Mouse Ports

The ATX PS/2 keyboard and the PS/2 mouse are located on J34. See Table 2-9 for pin definitions.

**Table 2-9**  
ATX PS/2 Keyboard and PS/2 Mouse Ports Pin Definitions for J34

Pin Number	Definition
1	Data
2	NC
3	Ground
4	VCC
5	Clock
6	NC

## Universal Serial Bus

The two Universal Serial Bus connectors are located on J17 and J18. See Table 2-10 for pin definitions.

**Table 2-10**  
Universal Serial Bus Pin Definitions  
J17 J18

Pin Number	Definition	Pin Number	Definition
1	+5V	1	+5V
2	P0-	2	P0-
3	P0+	3	P0+
4	Ground	4	Ground
5	N/A	5	Key

### ATX Serial Ports

ATX serial port COM1 is located on J20 and serial port COM2 is located on J21. See Table 2-11 for pin definitions.

**Table 2-11**  
ATX Serial Ports Pin Definitions  
J20 J21

Pin Number	Definition	Pin Number	Definition
1	DCD	6	CTS
2	DSR	7	DTR
3	Serial In	8	RI
4	RTS	9	Ground
5	Serial Out	10	NC

### CMOS Clear

Refer to Table 2-12 for instructions on how to clear the CMOS. **For an ATX power supply, you need to completely shut down the system, then use JBT1 to clear the CMOS. Do not use the PW\_ON connector to clear the CMOS.** A second way of resetting the CMOS contents is by depressing the <Ins> key, then turning on the system power. Release the key when the power comes on.

**Table 2-12**  
CMOS Clear Pin Definitions  
for Number JBT1

Jumper Position	Definition
1-2	Normal
2-3	CMOS Clear

The diagram shows a three-pin header with pins numbered 1, 2, and 3 from top to bottom. In the 'Normal' position, a jumper is placed over pins 1 and 2. In the 'CMOS Clear' position, a jumper is placed over pins 2 and 3.

### Wake-on-LAN

The Wake-on-LAN connector is located on WOL. Refer to Table 2-13 for pin definitions.

**Table 2-13**  
Wake-on-LAN Pin Definition located at WOL

Pin Number	Definition
1	+5V Standby
2	Ground
3	Wake up

### Fan Connectors\*

The thermal/overheat fan is located on JT3. The CPU fans are located on JT1 and JT2. Refer to Table 2-14 for pin definitions.

**Table 2-14**  
Fan Connectors Pin Definitions for JT1, JT2, JT3

Pin Number	Definition
1	Ground (black)
2	+12V (red)
3	Tachometer

\* Caution: These fan connectors are DC direct.

## Chassis Intrusion

The Chassis Intrusion Detector is located on JL1. See the board layouts in Chapter 1 and the PC Health Monitor section on page 1-15 for more information. See Table 2-15 for pin definitions.

**Table 2-15**  
Chassis Intrusion  
Detector Settings on  
JL1

Pin Number	Definition
1	Intrusion Input
2	Ground

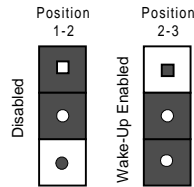
Open = Default, Close = Intrusion

## Keyboard Wake-Up

The Keyboard Wake-Up jumper is located on JPWAKE. To enable Keyboard Wake-Up, set the JPWAKE jumper to 2-3 and enable the Keyboard Wake-Up function in the system BIOS (see page 5-18 for more details). Refer to Table 2-16 for pin definitions.

**Table 2-16**  
Keyboard Wake-Up Pin  
Definitions for JPWAKE

Jumper Position	Definition
1-2	Disabled
2-3	Wake-Up Enabled



## Overheat LED

The Overheat LED connector is located on pins 1 and 2 of JOH. Refer to Table 2-17 for pin definitions.

**Table 2-17**  
Overheat LED Pin  
Definition for JOH

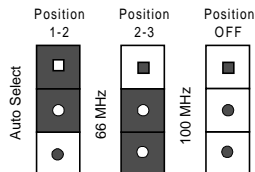
Pin Number	Definition
1	12V
2	OH Active

## Bus Speed

The Bus Speed jumper is located on JP11. **Note: Bus speed select (JP11) is not available on the 370SLA and 370SLM, which use the 440LX chipset.** Refer to Table 2-18 for instructions on setting the bus speed using jumper JP11. JP11 jumper setting 1-2 is the default setting. (*Note: Current Celeron processors only support a 66 MHz bus speed. Future Celeron processors may support a 100 MHz bus speed.*)

**Table 2-18**  
Bus Speed Pin  
Definitions for JP11

Jumper Position	Definition
1-2	Auto Select
2-3	66 MHz
OFF	100 MHz



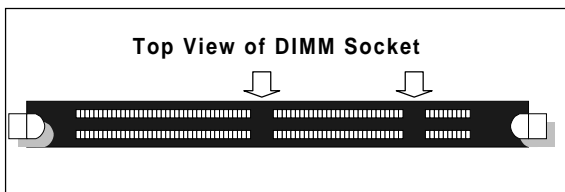
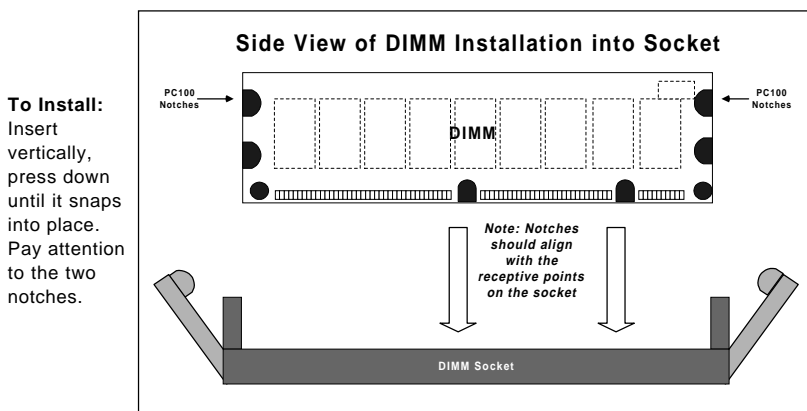
## 2-6 Installing DIMMs

### CAUTION

Exercise extreme care when installing or removing the DIMM modules to prevent any possible damage.

1. Insert DIMMs in Bank 0 through Bank 3 as required for the desired system memory.
2. Insert each DIMM module vertically into its socket. Pay attention to the two notches along the bottom of the module to prevent inserting the DIMM incorrectly.
3. Gently press the DIMM module until it snaps upright into place in the socket.
4. For best results, install DIMMs starting from Bank 0 (the DIMM socket farthest from the BX or LX chip).

Figure 2-1. DIMM Installation



## 2-7 Connecting Parallel, Floppy and Hard Disk Drives

Use the following information to connect the floppy and hard disk drive cables.

- The floppy disk drive cable has seven twisted wires.
- A red mark on a wire typically designates the location of pin 1.
- A single floppy disk drive ribbon cable has 34 wires and two connectors to provide for two floppy disk drives. The connector with twisted wires always connects to drive A, and the connector without twisted wires always connects to drive B.
- An IDE hard disk drive requires a data ribbon cable with 40 wires.
- A single IDE hard disk drive cable has two connectors to provide for two drives. To select an IDE disk drive as C, you would normally set the drive select jumper on the drive to DS1 (or Master). To select an IDE disk drive as D, you would normally set the drive select jumper on the drive to DS2 (or Slave). Consult the documentation that came with your disk drive for details on actual jumper locations and settings.

**Table 2-19**  
Parallel Port Pin Definitions for Connector J19

Pin Number	Function	Pin Number	Function
1	Strobe-	2	Auto Feed-
3	Data Bit 0	4	Error-
5	Data Bit 1	6	Init-
7	Data Bit 2	8	SLCT IN-
9	Data Bit 3	10	GND
11	Data Bit 4	12	GND
13	Data Bit 5	14	GND
15	Data Bit 6	16	GND
17	Data Bit 7	18	GND
19	ACK	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT	26	NC

## Parallel Port Connector

The parallel port is located on J19. See Table 2-19 for pin definitions.

**Table 2-20**  
Floppy Connector Pin Definitions for J22

Pin Number	Function	Pin Number	Function
1	GND	2	FDHDIN
3	GND	4	Reserved
5	Key	6	FDEDIN
7	GND	8	Index-
9	GND	10	Motor Enable
11	GND	12	Drive Select B-
13	GND	14	Drive Select A-
15	GND	16	Motor Enable
17	GND	18	DIR-
19	GND	20	STEP-
21	GND	22	Write Data-
23	GND	24	Write Gate-
25	GND	26	Track 00-
27	GND	28	Write Protect-
29	GND	30	Read Data-
31	GND	32	Side 1 Select-
33	GND	34	Diskette

## Floppy Connector

The floppy connector is located on J22. See Table 2-20 for pin definitions.

**Table 2-21**  
IDE Connector Pin Definitions

Pin Number	Function	Pin Number	Function
1	Reset IDE	2	GND
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	GND	20	Key
21	DRQ3	22	GND
23	I/O Write-	24	GND
25	I/O Read-	26	GND
27	IOCHRDY	28	BALE
29	DACK3-	30	GND
31	IRQ14	32	IOCS16-
33	Addr 1	34	GND
35	Addr 0	36	Addr 2
37	Chip Select 0	38	Chip Select 1-
39	Activity	40	GND

## IDE Interfaces

There are no jumpers to configure the onboard IDE interfaces J15 and J16. Refer to Table 2-21 for the pin definitions.



**Table 2-22**  
**AGP Port Pin Definitions for J8**

### AGP Port

There are no jumpers to configure the AGP port J8. Refer to Table 2-22 for the pin definitions.

Pin #	B	A	Pin #	B	A
1	Spare	12V	34	Vddq3.3	Vddq3.3
2	5.0V	Spare	35	AD21	AD22
3	5.0V	Reserved*	36	AD19	AD20
4	USB+	USB-	37	GND	GND
5	GND	GND	38	AD17	AD18
6	INTB#	INTA#	39	C/BE2#	AD16
7	CLK	RST#	40	Vddq3.3	Vddq3.3
8	REQ#	GNT#	41	IRDY#	Frame#
9	VCC3.3	VCC3.3	42		
10	ST0	ST1	43	GND	GND
11	ST2	Reserved	44		
12	RBF#	PIPE#	45	VCC3.3	VCC3.3
13	GND	GND	46	DEVSEL#	TRDY#
14	Spare	Spare	47	Vddq3.3	STOP#
15	SBA0	SBA1	48	PERR#	Spare
16	VCC3.3	VCC3.3	49	GND	GND
17	SBA2	SBA3	50	SERR#	PAR
18	SB_STB	Reserved	51	C/BE1#	AD15
19	GND	GND	52	Vddq3.3	Vddq3.3
20	SBA4	SBA5	53	AD14	AD13
21	SBA6	SBA7	54	AD12	AD11
22	KEY	KEY	55	GND	GND
23	KEY	KEY	56	AD10	AD9
24	KEY	KEY	57	AD8	C/BE0#
25	KEY	KEY	58	Vddq3.3	Vddq3.3
26	AD31	AD30	59	AD_STB0	Reserved
27	AD29	AD28	60	AD7	AD6
28	VCC3.3	VCC3.3	61	GND	GND
29	AD27	AD26	62	AD5	AD4
30	AD25	AD24	63	AD3	AD2
31	GND	GND	64	Vddq3.3	Vddq3.3
32	AD_STB1	Reserved	65	AD1	AD0
33	AD23	C/BE3#	66	SMB0	SMB1

**Notes**

## Chapter 3 Troubleshooting

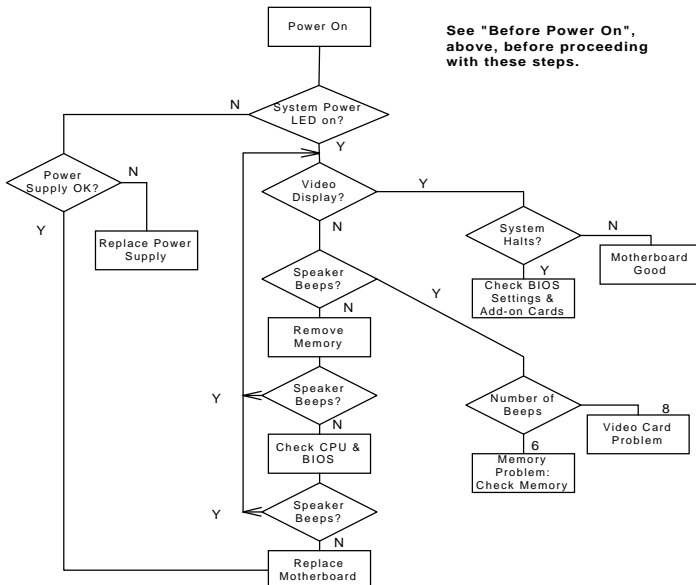
### 3-1 Troubleshooting Procedures

Use the following procedures and chart to troubleshoot your system. If you have followed all of the procedures below and still need assistance, refer to the 'Technical Support Procedures' and/or 'Returning Merchandise for Service' section(s) in this chapter.

#### Before Power On

1. Make sure no short circuits exist between the motherboard and chassis.
2. Disconnect all ribbon/wire cables from the motherboard.
3. Remove all add-on cards except the video/graphics card. (Be sure the video/graphics card is inserted properly.)
4. Install a CPU, the chassis speaker and the power LED to the motherboard. (Check all the jumper settings as well.)
5. Install a memory module into Bank 0.
6. Check the power supply voltage monitor 115V/230V switch.

**Figure 3-1. Troubleshooting Flowchart**



### **No Power**

1. Make sure that the default jumper is on and the CPU is correctly set up.
2. Turn the power switch on and off to test the system.
3. If changing the jumper setting has not helped, clear CMOS.
4. Check the power supply voltage monitor. (Check the power supply 115V/230V switch.)

### **No Video**

Use the following steps to troubleshoot your system configuration.

1. If the power is on but you have no video, remove all the add-on cards and cables.
2. Check for shorted connections, especially under the motherboard.
3. Check the jumpers settings, clock speed and voltage settings.
4. Use the speaker to determine if any beep codes exist. Refer to Appendix A for details on beep codes.

---

### **NOTE**

If you are a system integrator, VAR or OEM, a POST diagnostics card is recommended. For port 80h codes, refer to Appendix B.

---

### **Memory Errors**

If you encounter memory error, follow the procedures below.

1. Check to determine if the DIMM modules are improperly installed.
2. Make sure that different types of DIMMs have not been installed in different banks (e.g., a mixture of 2MB x 36 and 1 MB x 36 DIMMs in Bank 0).
3. Determine if different speeds of DIMMs have been installed and verify that the BIOS setup is configured for the fastest speed of RAM used. It is recommended to use the same RAM speed for all DIMMs in the system.
4. Check for bad DIMM modules or chips.
5. Try to install the minimum amount of memory first (a single bank).

### **Losing the System's Setup Configuration**

1. Check the setting of jumper JBT1. Ensure that you are using a high quality power supply. A poor quality power supply may cause the

system to lose the CMOS setup information. Refer to Chapter 1 of this manual for details.

2. If the above step does not fix the setup configuration problem, contact your vendor for repairs.

## 3-2 Technical Support Procedures

1. Please go through the 'Troubleshooting Procedures' and 'Frequently Asked Question' (FAQ) sections in this chapter of the manual or check our web site FAQ ([http:// www.supermicro.com](http://www.supermicro.com)) before contacting Technical Support.
2. Take note that as a motherboard manufacturer, Super Micro does not sell directly to end-users, so it is best to check with your distributor or reseller for troubleshooting services. They should know of any possible problem(s) with the specific system configuration that was sold to you.
3. BIOS upgrades can be downloaded from the SUPER BBS# (408) 895-2022, 24 hours a day, using 1200-28800 baud, 8 data bits, 1 stop bit and no parity. BIOS upgrades can also be downloaded from our web site at [http:// www.supermicro.com](http://www.supermicro.com).

*Note: Not all BIOS can be flashed depending on the modifications to the boot block code.*

4. If you still cannot resolve the problem, include the following information when you e-mail Super Micro for technical support:
  - BIOS release date/version
  - System board serial number
  - Product model name
  - Invoice number and date
  - System configuration

Due to the volume of e-mail we receive and the time it takes to replicate problems, a response to your question may not be immediately available. Please understand that we do not have the resources to serve every end-user, however we will try our best to help all our customers.

5. Distributors: For immediate assistance, please have your account number ready when placing a call to our technical support department.

### 3-3 Frequently Asked Questions

**Question:** What are the differences between the various memories that the 370SBA/370SBM/370SLA/370SLM motherboard can support?

**Answer:** The 370SBA/370SBM integrates a main memory DRAM controller that supports 64-bit or 72-bit (64 bits of memory data plus 8 ECC bits) DRAM from 8 MB to 512 MB for SDRAM and from 8 MB to 768 MB for EDO or registered DIMMs. The DRAM types supported are either Extended Data Out (EDO), Synchronous DRAM (SDRAM) or registered DIMM modules.

**Note:** EDO DIMMs are not recommended for running 100 MHz bus speed.

1. Mixing ECC and non-ECC will result in non-ECC operation. EC/ECC is supported properly in the 440BX, only if all the memory is 72 bits wide. A system with a mixture of 64 and 72-bit wide memory will disable the ECC mode.
2. EDO memory and SDRAM cannot be mixed.
3. Registered SDRAM and unbuffered SDRAM cannot be mixed.
4. Mixing PC/100 DIMM and PC/66 DIMM will result in an unexpected memory count or system errors.
5. User should populate the DIMMs starting with the DIMM socket located the furthest from the BX chip.
6. If EDO memory is used, the CPU bus should be set at 66 MHz Bus speed only.

**Question:** How do I update my BIOS?

**Answer:** It is recommended that you **do not** upgrade your BIOS if you are experiencing no problems with your system. BIOS file updates are located on our web site at [http:// www.supermicro.com](http://www.supermicro.com). Please check the current BIOS revision and make sure it is newer than your BIOS before downloading. Select your motherboard model and download the BIOS file to your computer. Unzip the BIOS update file and you will find the readme.txt (flash instructions), the sm2flash.com (BIOS flash utility), and the BIOS image (xxxxxx.rom) files. Copy these files onto a bootable floppy and reboot your system. It is not necessary to set BIOS boot block protection jumpers on the motherboard. At the DOS prompt, enter the command "sm2flash." This will start the flash utility and give you an opportunity to save your current BIOS image. Flash the boot block and enter the name of the update BIOS image file. NOTE: It is important to save your current BIOS and rename it "super.rom" in case you need to recover from a failed BIOS update. Select flash boot block, then enter the update BIOS image. Select

"Y" to start the BIOS flash procedure and do not disturb your system until the flash utility displays that the procedure is complete. After updating your BIOS, clear CMOS then load Optimal Values in the BIOS.

**Question: After flashing the BIOS my system does not have video. How can I correct this?**

**Answer:** If the system does not have video after flashing your new BIOS, it indicates that the flashing procedure failed. To remedy this, first clear CMOS per the instructions in this manual and retry the BIOS flashing procedure. If you still do not have video, please use the following BIOS recovery procedure. Turn your system off and place the floppy disk with the saved BIOS image file (see above FAQ) in drive A. Press and hold <CTRL> and <Home> at the same time, then turn on the power with these keys pressed until your floppy drive starts reading. Your screen will remain blank until the BIOS program is done. If the system reboots correctly, then the recovery was successful.

**Question: I have memory problems. What is the correct memory to use and which BIOS setting should I choose?**

**Answer:** The correct memory to use on the SUPER 370SBA/370SBM/370SLA/370SLM is 168-pin DIMM 3.3v non-buffered SPD (Serial Present Detection) SDRAM, SDRAM and EDO memory. SPD SDRAM is preferred but is not essential. IMPORTANT: Please do not mix memory types; the results are unpredictable. If your memory count is exactly half of the correct value, please go to the BIOS in Chipset Setup and set "SDRAM AUTOSIZING SUPPORT" to *Enabled*. Change between available options until one setting correctly displays your memory.

**Question: Which Operating System (OS) supports AGP?**

**Answer:** At present, Windows 98 and Windows NT 5.0 are the only OS that have built-in support for AGP. Some AGP video adapters can run Windows 95 OSR2.1 with special drivers. Please contact your graphics adapter vendor for more details.

**Question: Do I need the CD that came with your motherboard?**

**Answer:** The supplied compact disc has quite a few drivers and programs that will greatly enhance your system. We recommend that you review the CD and install the applications you need. Applications included on the CD are PCI IDE Bus Master drivers for Windows 95 and Windows NT, 440BX/LX chip set drivers for Windows 95 and Super Doctor Monitoring software.

**Question:** Why can't I turn off the power using the momentary power on/off switch?

**Answer:** The instant power off function is controlled by the BIOS. When this feature is enabled in the BIOS, the motherboard will have instant off capabilities as long as the BIOS has control of the system. When this feature is disabled or when the BIOS is not in control, such as during memory count (the first screen that appears when the system is turned on), the momentary on/off switch must be held for more than four seconds to shut down. This feature is required to implement the ACPI features on the motherboard.

**Question:** I see some of my PCI devices sharing IRQs, but the system seems to be fine. Is this correct or not?

**Answer:** Some PCI Bus Mastering devices can share IRQs without performance penalties. These devices are designed to work correctly while sharing IRQs.

### 3-4 Returning Merchandise for Service

A receipt or copy of your invoice marked with the date of purchase is required before any warranty service will be rendered. You can obtain service by calling your vendor for a Returned Merchandise Authorization (RMA) number. When returning to the manufacturer, the RMA number should be prominently displayed on the outside of the shipping carton, and mailed prepaid or hand-carried. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

This warranty only covers normal consumer use and does not cover damages incurred in shipping or from failure due to the alternation, misuse, abuse or improper maintenance of products.

During the warranty period, contact your distributor first for any product problems.



# Chapter 4

## AMIBIOS

### 4-1 Introduction

This chapter describes the AMIBIOS for the Intel 440LX/BX Celeron 333-400 MHz processors. The AMI ROM BIOS is stored in the Flash EEPROM and is easily upgraded using a floppy disk-based program.

#### **System BIOS**

The BIOS is the Basic Input Output System used in all IBM® PC, XT™, AT®, and PS/2® compatible computers. WinBIOS is a high-quality example of a system BIOS.

#### **Configuration Data**

AT-compatible systems, also called ISA (Industry Standard Architecture) must have a place to store system information when the computer is turned off. The original IBM AT had 64k bytes of non-volatile memory storage in CMOS RAM. All AT-compatible systems have at least 64k bytes of CMOS RAM, which is usually part of the Real-Time Clock. Many systems have 128k bytes of CMOS RAM.

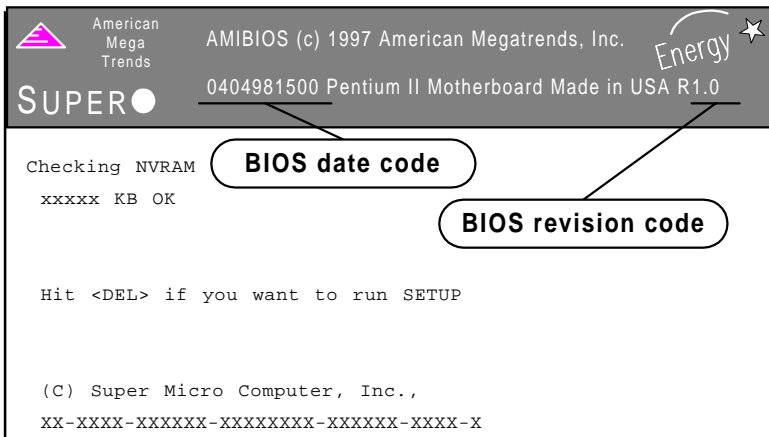
#### **How Data Is Configured**

AMIBIOS provides a Setup utility in ROM that is accessed by pressing <Del> at the appropriate time during system boot. Setup configures data in CMOS RAM.

#### **POST Memory Test**

Normally, the only visible POST routine is the memory test. The screen that appears when the system is powered on is shown on the next page.

An AMIBIOS Identification string is displayed at the left bottom corner of the screen, below the copyright message.



## 4-2 BIOS Features

The AMIBIOS:

- Supports Plug and Play V1.0A and DMI 2.1
- Supports Intel PCI 2.1 (Peripheral Component Interconnect) local bus specification
- Supports Advanced Power Management (APM) specification v 1.1
- Supports xACP2
- Supports Flash ROM.

AMIBIOS supports the LS120 drive made by Matsushita-Kotobuki Electronics Industries Ltd. The LS120:

- Can be used as a boot device
- Is accessible as the next available floppy drive.

AMIBIOS supports PC Health Monitoring chips. When a failure occurs in a monitored activity, AMIBIOS can sound an alarm and display a message. The PC Health Monitoring chips monitor:

- CPU temperature
- Additional temperature sensors
- Chassis intrusion detector
- Five positive voltage inputs
- Two negative voltage inputs
- Three fan speed monitoring inputs.

## BIOS Configuration Summary Screen

AMIBIOS displays a screen that looks similar to the following when the POST routines complete successfully.

AMIBIOS System Configuration (C) 1985-1997 American Megatrends Inc.,			
Main Processor	: Pentium(tm) II	Base Memory Size	: 640 KB
Math Processor	: Built-In	Ext. Memory Size	: 64512 KB
Floppy Drive A:	: 1.44 MB, 3 <sup>1</sup> / <sub>2</sub>	Display Type	: VGA/EGA
Floppy Drive B:	: None	Serial Port(s)	: 3F8, 2F8
AMI-BIOS Date	: 7/15/95	Parallel Port(s)	: 378
Processor Clock	: 350MHz	External Cache	: 512 KB
PCI Devices			
PCI Onboard PCI Bridge		PCI Onboard Bridge Device	
PCI Onboard USB Controller		PCI Onboard IDE	
PCI Onboard SCSI, IRQ 10		PCI Onboard SCSI, IRQ 10	
PCI Slot 4 VGA, IRQ 11			

\*Note: The picture above reflects a board equipped with SCSI, but may be taken as a general example.

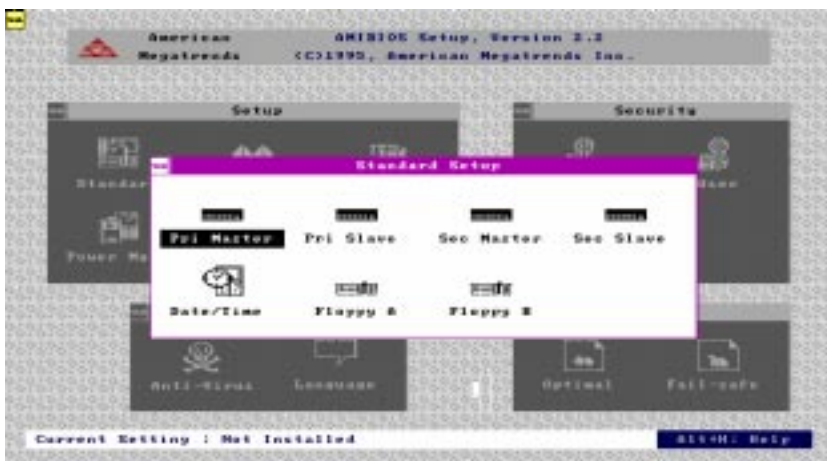
## AMIBIOS Setup

See the following page for examples of the AMIBIOS Setup screen, featuring options and settings. Figure 4-1 shows the **Standard** option highlighted. To highlight other options, use the arrow keys or the tab key to move to other option boxes. Figure 4-2 shows the settings for the Standard setup. Settings can be viewed by highlighting a desired option and pressing <Enter>. Use the arrow keys to choose a setting. Note: Optimal settings for all options can be set automatically. Go to the **Optimal** icon in the default box and press <Enter>. Use the arrow keys to highlight yes, then press <Enter>.

Figure 4-1. Standard Option Highlighted



Figure 4-2. Settings for Standard Option



## Chapter 5 Running Setup

*Optimal and Fail-Safe default settings are in bold text unless otherwise noted.*

The WinBIOS Setup options described in this section are selected by choosing the appropriate high-level icon from the Standard Setup screen. All displayed icons are described in this section, although the screen display is often all you need to understand how to set the options. *Note: The 370S\* motherboards are running AMIBIOS Setup, Version 2.5 © 1997.*

### 5-1 Setup

#### Standard Setup

*Pri Master*

*Pri Slave*

*Sec Master*

*Sec Slave*

*Date/Time*

*Floppy A*

*Floppy B*

Select these options to configure the drive named in the option. Select *Auto Detect IDE* to let AMIBIOS automatically configure the drive. A screen with a list of drive parameters appears. Click on *OK* to configure the drive.

#### Type

#### How to Configure

#### **IDE**

Select *Type*. Select *Auto* to let AMIBIOS determine the parameters. Click on *OK* when AMIBIOS displays the drive parameters. Select *LBA Mode*. Select *On* if the drive has a capacity greater than 540 MB. Select the *Block Mode*. Select *On* to allow block mode data transfers. Select the *32-bit mode*. Select *On* to allow 32-bit data transfers. Select *PIO mode*. Select *On* to allow AMIBIOS to determine the PIO Mode. It is best to select *Auto* to allow AMIBIOS to determine the PIO mode. If you select a PIO mode that is not supported by the IDE drive, the drive will not work properly. If you are absolutely certain that you know the drive's PIO mode, select PIO mode 0-4, as appropriate.

**SCSI** Select *Type*. Select *Not Installed* on the drive parameter screen. The SCSI drivers provided by the SCSI manufacturer should allow you to configure the SCSI drive.

**IDE CDROM** Select *Type*: Select *ATAPI CDROM* on the drive parameter screen. ATAPI CDROM enables ATAPI-compliant IDE CD-ROM drives to be automatically configured. Select *Auto* for PIO Mode to let AMIBIOS configure IDE CD-ROM drives.

**Removable Media Drive** Select *Type*: Select *ARMD* on the drive parameter screen. ATAPI Removal Media Device (ARMD) enables removable media drives to be configured. Select *Auto* for PIO Mode to let AMIBIOS emulate LS120 as a floppy, Iomega ZIP as a hard drive, and MO as a hard drive.

### **Entering Drive Parameters (User Defined)**

You can also enter the hard disk drive parameters. The drive parameters are:

Parameter	Description
Type	The number for a drive with certain identification parameters.
Cylinders	The number of cylinders in the disk drive.
Heads	The number of heads.
Write Precompensation	The size of a sector gets progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. Write precompensation circuitry on the hard disk compensates for the physical difference in sector size by boosting the write current for sectors on inner tracks. This parameter is the track number where write precompensation begins.
Sectors	The number of sectors per track. MFM drives have 17 sectors per track. RLL drives have 26 sectors per track. ESDI drives have 34 sectors per track. SCSI and IDE drive may have even more sectors per track.
Capacity	The formatted capacity of the drive is (Number of heads) x (Number of cylinders) x (Number of sectors per track) x (512 bytes per sector)

**Date and Time Configuration**

Select the Standard option. Select the *Date/Time* icon. The current values for each category are displayed. Enter new values through the keyboard.

**Floppy A****Floppy B**

Choose the Floppy Drive A or B icon to specify the floppy drive type. The settings are *Not Installed*, *360 KB 5¼ inch*, *1.2 MB 5¼ inch*, *720 KB 3½ inch*, *1.44 MB 3½ inch* or *2.88 MB 3½ inch*. **Note: The Optimal and Fail-Safe settings for Floppy Drive A are 1.44 MB 3 1/2 inch and for Floppy Drive B are Not Installed.**

**Advanced Setup****Quick Boot**

The Settings are **Disabled** or **Enabled**. Set to **Enabled** to permit AMIBIOS to boot quickly when the computer is powered on. This option replaces the old Above 1 MB Memory Test Advanced Setup option. The settings are:

<u>Setting</u>	<u>Description</u>
<b>Disabled</b>	AMIBIOS tests all system memory. AMIBIOS waits up to 40 seconds for a READY signal from the IDE hard disk drive. AMIBIOS waits for .5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again. AMIBIOS checks for a <Del> key press and runs AMIBIOS Setup if the key has been pressed.
<b>Enabled</b>	AMIBIOS does not test system memory above 1 MB. AMIBIOS does not wait up to 40 seconds for a READY signal from the IDE hard disk drive. If a READY signal is not received immediately from the IDE drive, AMIBIOS does not configure that drive. AMIBIOS does not wait for .5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again. In <b>Enabled</b> , keyboard will be bypassed.

**Note: You cannot run AMIBIOS Setup at system boot, because there is no delay for the Hit <Del> to run Setup message.**

***Pri Master ARMD Emulated as******Pri Slave ARMD Emulated as******Sec Master ARMD Emulated as******Sec Slave ARMD Emulated as***

Options for Pri Master ARMD Emulated as, Pri Slave ARMD Emulated as, Sec Master ARMD Emulated as and Sec Slave ARMD Emulated as are **Auto**, **Floppy** or **Hard disk**.

***1st Boot Device******2nd Boot Device******3rd Boot Device***

The options for 1st Boot Device are *Disabled*, *1st IDE-HDD*, *2nd IDE-HDD*, *3rd IDE-HDD*, *4th IDE-HDD*, **Floppy**, **ARMD-FDD**, **ARMD-HDD**, **ATAPI CD ROM**, **SCSI**, **Network** or **I<sub>2</sub>O**. The options for 2nd Boot Device are *Disabled*, **1st IDE-HDD**, *2nd IDE-HDD*, *3rd IDE-HDD*, *4th IDE-HDD*, **Floppy**, **ARMD-FDD**, **ARMD-HDD** or **ATAPI CD ROM**. The options for 3rd Boot Device are *Disabled*, *1st IDE-HDD*, *2nd IDE-HDD*, *3rd IDE-HDD*, *4th IDE-HDD*, **Floppy**, **ARMD-FDD**, **ARMD-HDD** or **ATAPI CD ROM**.

1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD and 4th IDE-HDD are the four hard disks that can be installed by the BIOS. 1st IDE-HDD is the first hard disk installed by the BIOS, 2nd IDE-HDD is the second hard disk, and so on. For example, if the system has a hard disk connected to Primary Slave and another hard disk to Secondary Master, then 1st IDE-HDD will be referred to as the hard disk connected to Primary Slave and 2nd IDE-HDD will be referred to as the hard disk connected to the Secondary Master. 3rd IDE-HDD and 4th IDE-HDD are not present. Note that the order of the initialization of the devices connected to the primary and secondary channels are Primary Master first, Primary Slave second, Secondary Master third, and Secondary Slave fourth.

The BIOS will attempt to read the boot record from 1st, 2nd, 3rd and 4th boot device in the selected order until it is successful in reading the booting record. The BIOS will not attempt to boot from any device which is not selected as the boot device.

***Try Other Boot Device***

This option controls the action of the BIOS if all the selected boot devices failed to boot. The settings for this option are **Yes** or **No**. If **Yes** is selected and all the selected boot devices failed to boot, the BIOS will try to boot from the other boot devices (in a predefined sequence) which are present but not selected as boot devices in the setup (and hence not yet



been tried for booting). If selected as *No* and all selected boot devices failed to boot, the BIOS will try not to boot from the other boot devices which may be present but not selected as boot devices in setup.

#### ***Initial Display Mode***

This option determines the display screen with which the POST is going to start the display. The settings for this option are ***BIOS*** or ***Silent***. If selected as ***BIOS***, the POST will start with the normal sign-on message screen. If ***Silent*** is selected, the POST will start with the silent screen.

#### ***Display Mode at Add-on ROM Init***

This option determines the display mode during add-on ROM (except Video add-on ROM) initialization. The settings for this option are ***Force BIOS*** or ***Keep Current***. If selected as ***Force BIOS***, the POST will force the display to be changed to BIOS mode before giving control to any add-on ROM. If no add-on ROM is found, then the current display mode will remain unchanged even if this setup question is selected as ***Force BIOS***. If selected as ***Keep Current***, then the current display mode will remain unchanged.

#### ***Floppy Access Control***

The settings for this option are ***Read-Write*** or ***Read-Only***.

#### ***Hard Disk Access Control***

The settings for this option are ***Read-Write*** or ***Read-Only***.

#### ***S.M.A.R.T. for Hard Disks***

S.M.A.R.T. (Self-Monitoring, Analysis and Reporting Technology) is a technology developed to manage the reliability of the hard disk by predicting future device failures. The hard disk needs to be S.M.A.R.T. capable. The settings for this option are ***Disabled*** or ***Enabled***. **Note: S.M.A.R.T. cannot predict all future device failures. S.M.A.R.T. should be used as a warning tool, not as a tool to predict the device reliability.**

#### ***Boot Up Num-Lock***

Settings for this option are ***On*** or ***Off***. When this option is set to ***On***, the BIOS turns off the Num Lock key when the system is powered on. This will enable the end user to use the arrow keys on both the numeric keypad and the keyboard.

#### ***PS/2 Mouse Support***

Settings for this option are ***Enabled*** or ***Disabled***. When this option is set to ***Enabled***, AMIBIOS supports a PS/2-type mouse.

**Primary Display**

This option specifies the type of display adapter card installed in the system. The settings are *Absent*, **VGA/EGA**, *CGA40x25*, *CGA80x25* or *Mono*.

**Password Check**

This option enables the password check option every time the system boots or the end user runs WinBIOS Setup. If *Always* is chosen, a user password prompt appears every time the computer is turned on. If **Setup** is chosen, the password prompt appears if WinBIOS Setup is executed.

**Boot to OS/2**

If DRAM size is over 64 MB, set this option to *Yes* to permit AMIBIOS to run with IBM OS/2. The settings are **No** or *Yes*.

**Internal Cache**

This option is for enabling or disabling the internal cache memory. The settings for this option are *Disabled*, *WriteThru*, or **WriteBack**.

**System BIOS Cacheable**

When set to *Enabled*, the contents of the F0000h system memory segment can be read from or written to cache memory. The contents of this memory segment are always copied from the BIOS ROM to system RAM for faster execution. The settings are *Enabled* or *Disabled*. **Note: The Optimal default setting is Enabled and the Fail-Safe default setting is Disabled. Set this option to Enabled to permit the contents of F0000h RAM memory segment to be written to and read from cache memory.**

**CPU ECC**

This option is *grayed out* for the Celeron processor, but is available for the Pentium II L2 cache ECC function.

**C000, 16K Shadow****C400, 16K Shadow**

(370S\* motherboard defaults are C000:Enabled, C400:Cached.) These options specify how the 32 KB of video ROM at C0000h and C4000h is treated. The settings are: *Disabled*, **Enabled** or **Cached**. When set to *Disabled*, the contents of the video ROM are not copied to RAM. When set to *Enabled*, the contents of the video ROM area from C0000h-C7FFFh are copied (shadowed) from ROM to RAM for faster execution. When set to *Cached*, the contents of the video ROM area from C0000h-C7FFFh are copied from ROM to RAM, and can be written to or read from cache memory.

**C800, 16K Shadow**

**CC00, 16K Shadow**

**D000, 16K Shadow**

**D400, 16K Shadow**

**D800, 16K Shadow**

**DC00, 16K Shadow**

These options enable shadowing of the contents of the ROM area named in the option. The ROM area not used by ISA adapter cards is allocated to PCI adapter cards. The settings are: **Disabled**, **Enabled** or **Cached**. When set to **Disabled**, the contents of the video ROM are not copied to RAM. When set to **Enabled**, the contents of the video ROM area from C0000h-C7FFFh are copied (shadowed) from ROM to RAM for faster execution. When set to **Cached**, the contents of the video ROM area from C0000h-C7FFFh are copied from ROM to RAM and can be written to or read from cache memory.

## Chipset Setup

### **USB Function**

The settings for this option are **Enabled** or **Disabled**. Set this option to **Enabled** to enable the USB (Universal Serial Bus) functions.

### **USB KB/Mouse Legacy Support**

The settings for this option are **Keyboard**, **Auto**, **Keyboard+Mouse** or **Disabled**. Set this option to **Enabled** to enable the USB keyboard and mouse.

### **Port 64/60 Emulation**

The settings for this option are **Enabled** or **Disabled**. Set this option to **Enabled** to enable the USB (Universal Serial Bus) functions.

### **SERR# (System Error)**

The settings for this option are **Enabled** or **Disabled**. Set to **Enabled** to enable the SERR# signal on the bus. BX asserts this signal to indicate a system error condition. SERR# is asserted under the following conditions:

- In an ECC configuration, the 82443BX asserts SERR#, for single bit (correctable) ECC errors or multiple bit (non-correctable) ECC errors if SERR# signaling is enabled via the ERRCMD control register. Any ECC errors received during initialization should be ignored.
- The 82443BX asserts SERR# for one clock when it detects a target abort during 82443BX initiated PCI cycle.
- The 82443BX can also assert SERR# when a PCI parity error occurs during the address or data phase.
- The 82443BX can assert SERR# when it detects a PCI address or data parity error on AGP.
- The 82443BX can assert SERR# upon detection of access to an invalid entry in the Graphics Aperature Translation Table.

- The 82443BX can assert SERR# upon detecting an invalid AGP master access outside of AGP aperture and outside of main DRAM range (i.e., in the 640k - 1M range or above TOM).
- The 82443BX can assert SERR# upon detecting an invalid AGP master access outside of AGP aperture.
- The 82443BX asserts SERR# for one clock when it detects a target abort during 82443BX initiated AGP cycle.

### **PERR#**

This option signals data parity errors of the PCI bus. The settings are *Enabled* or **Disabled**. Set to *Enabled* to enable the PERR# signal.

### **WSC# Handshake (Write Snoop Complete)**

This signal is asserted active to indicate that all the snoop activity on the CPU bus on the behalf of the last PCI-DRAM write transaction is complete and that it is safe to send the APIC interrupt message. The settings for this option are **Enabled** or *Disabled*. Set to *Enabled* to enable handshaking for the WSC# signal.

### **USWC Write Post**

The settings for this option are **Enabled** or *Disabled*. This option sets the status of USWC (Uncacheable, Speculative, Write-Combining) posted writes and is used to combine several partial writes to the frame buffer into a single write in order to reduce the data bus traffic. Set to *Enabled* to enable USWC posted writes to I/O. Set to *Disabled* to disable USWC posted writes to I/O.

### **BX/GX Master Latency Timer (CLKs)**

This option specifies the master latency timings (in PCI clocks) for devices in the computer. It defines the number of PCI clocks a PCI master can own on the bus after PCI central arbiter removes the grant signal. The settings are *Disabled*, 32, **64**, 96, 128, 160, 192 or 224.

### **Multi-Trans Timer (Clks)**

This option specifies the multi-trans latency timings (in PCI clocks) for devices in the computer. It reduces overhead switching between different masters. The settings are *Disabled*, **32**, 64, 96, 128, 160, 192 or 224.

### **PCI1 to PCI0 Access**

PCI1 refers to AGP in BX and LX chipsets. PCI0 is the normal PCI bus.

**Note: Normally AGP master should not access to a PCI target.** The settings for this option are *Enabled* or **Disabled**. Set to *Enabled* to enable access between two different PCI buses (PCI1 and PCI0).

**Memory Autosizing Support**

The dynamic detection and sizing of SDRAM and EDO is performed by the BIOS in a system populated with memory which has no SPD information. When set to *Enable*, memory does not have the SPD information. The settings for this option are **Auto** or *Enable*.

**DRAM Integrity Mode**

This option is *grayed out* for the Celeron processor, but is available for the Pentium II processor.

**DRAM Refresh Rate**

This option specifies the interval between Refresh signals to DRAM system memory. The settings for this option are **15.6 us** (micro-seconds), *31.2 us*, *62.4 us*, *124.8 us* or *249.6 us*.

**Memory Hole**

This option specifies the location of an area of memory that cannot be addressed on the ISA bus. The settings are **Disabled**, *15 MB-16 MB*, or *512 KB-640 KB*.

**SDRAM CAS# Latency**

This option regulates the column address strobe. The settings are 2 SCLKs, 3 SCLKs or **Auto**.

**SDRAM RAS# to CAS# Delay**

This option specifies the length of the delay inserted between the RAS and CAS signals of the DRAM system memory access cycle if SDRAM is installed. The settings are *Auto* (AMIBIOS automatically determines the optimal delay), *2 SCLKs* or *3 SCLKs*. **Note: The Optimal default setting is Auto and the Fail-Safe default setting is 3 SCLKs.**

**SDRAM RAS# Precharge**

This option specifies the length of the RAS precharge part of the DRAM system memory access cycle when Synchronous DRAM system memory is installed in the computer. The settings are *Auto* (AMIBIOS automatically determines the optimal delay), *2 SCLKs* or *3 SCLKs*. **Note: The Optimal default setting is Auto and the Fail-Safe default setting is 3 SCLKs.**

**Power Down SDRAM**

BX supports SDRAM power down mode to minimize SDRAM power usage. The settings for this option are *Enabled* or **Disabled**. The *Enabled* setting enables the SDRAM Power Down feature.

**ACPI Control Register**

The settings for this option are *Enabled* or *Disabled*. Set this option to *Enabled* to enable the ACPI (Advanced Configuration and Power Interface) control register.

**Gated Clock**

Signal GCLKEN enables internal dynamic clock gating in the 82443BX when a AGPset "IDLE" state occurs. This happens when the 82443BX detects an idle state on all its buses. The settings for this option are *Enabled* or *Disabled*. The *Enabled* setting enables the gated clock.

**Graphics Aperture Size**

This option specifies the amount of system memory that can be used by the Accelerated Graphics Port (AGP). The settings are 4 MB, 8 MB, 16 MB, 32 MB, **64 MB**, 128 MB, or 256 MB.

**Search for MDA (Monochrome Adapter) Range (B0000h-B7FFFh) Resources**

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. In an AGP system, accesses in the normal VGA range are forwarded to the AGP bus. Since the monochrome adapter may be on the PCI (or ISA) bus, the 82443BX must decode cycles in the MDA range and forward them to PCI. The settings for this option are **Yes** or *No*. Set this option to **Yes** to let AMIBIOS search for MDA resources.

**AGP Multi-Trans Timer (AGP Clks)**

This option sets the AGP multi-trans timer. The settings are in units of AGP clocks: **32**, 64, 96, 128, 160, 192, or 224.

**AGP Low-Priority Timer**

This option controls the minimum tenure on the AGP for low priority data transaction for both read and write. The settings are *Disabled*, 16, **32**, 48, 64, 80, 96, 112, 128, 144, 176, 192, 208, 224, or 240.

**AGP SERR (Advanced Graphic Port System Error)**

BX asserts this signal to indicate a AGP system error condition. The settings for this option are *Enabled* or *Disabled*. Set to *Enabled* to enable the AGP SERR# signal.

**AGP Parity Error Response**

The settings for this option are *Enabled* or **Disabled**. Set to *Enabled* to enable the AGP (Accelerated Graphics Port) to respond to parity errors.

**8bit I/O Recovery Time**

This option specifies the length of a delay inserted between consecutive 8-bit I/O operations. The settings are **Disabled**, 1 SYSCALL, 2 SYSCALLs, 3 SYSCALLs, 4 SYSCALLs, 5 SYSCALLs, 6 SYSCALLs, 7 SYSCALLs or 8 SYSCALLs.

**16bit I/O Recovery Time**

This option specifies the length of a delay inserted between consecutive 16-bit I/O operations. The settings are **Disabled**, 1 SYSCALL, 2 SYSCALLs, 3 SYSCALLs, or 4 SYSCALLs.

**PIIX4 SERR#**

This signal is asserted to indicate a PIIX4 System Error condition. The settings for this option are *Enabled* or **Disabled**. The *Enabled* option enables the SERR# signal for the Intel PIIX4 chip.

**USB Passive Release**

BX releases USB bus when it is idle to maximize the USB bus usage. The settings for this option are **Enabled** or *Disabled*. Set this option to *Enabled* to enable passive release for USB.

**PIIX4 Passive Release**

This option functions similarly to USB Passive Release. The settings for this option are **Enabled** or *Disabled*. Set to *Enabled* to enable passive release for the Intel PIIX4 chip.

**PIIX4 Delayed Transaction**

BX is capable of PIIX4 transaction to improve PIIX4 interrupt efficiency. The settings for this option are **Enabled** or *Disabled*. Set this option to *Enabled* to enable delayed transactions for the Intel PIIX4 chip.

**Type F DMA Buffer Control1****Type F DMA Buffer Control2**

These options specify the DMA channel where Type F buffer control is implemented. The settings are **Disabled**, *Channel-0*, *Channel-1*, *Channel-2*, *Channel-3*, *Channel-4*, *Channel-5*, *Channel-6* or *Channel-7*.

**DMA0 Type****DMA1 Type****DMA2 Type****DMA3 Type****DMA5 Type****DMA6 Type****DMA7 Type**

These options specify the bus that the specified DMA channel can be used on. The settings are *PC/PCI*, *Distributed*, or **Normal ISA**.

**Memory Buffer Strength**

The settings for this option are *Strong*, *Median*, or **Auto**.

**Manufacturer's Setting**

Modes 0 through 4 are available. **Note: The user should always set this option to mode 0. All other modes are for factory testing only.**

## Power Management

**Power Management**

The settings for this feature are: **APM** or *Disabled*. Set to **APM** to enable the power conservation feature specified by Intel and Microsoft INT 15h Advance Power Management BIOS functions.

**Power Button Function**

This option specifies how the power button mounted externally on the computer chassis is used. The settings are: *Suspend* or **On/Off**. When set to *On/Off*, pushing the power button turns the computer on or off. When set to *Suspend*, pushing the power button places the computer in Suspend mode or Full On power mode.

**Green PC Monitor Power State**

This option specifies the power state that the green PC-compliant video monitor enters when AMIBIOS places it in a power savings state after the specified period of display inactivity has expired. The settings are *Standby*, *Suspend* or *Off*. **Note: The Optimal default setting for this option is Suspend and the Fail-Safe setting is Standby.**

**Video Power Down Mode**

This option specifies the power conserving state that the VGA video subsystem enters after the specified period of display inactivity has expired. The settings are *Disabled*, *Standby*, or *Suspend*. **Note: The Optimal default setting for this option is Suspend and the Fail-Safe default setting is Disabled.**



**Hard Disk Power Down Mode**

This option specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired. The settings are *Disabled*, *Standby*, or *Suspend*. **Note: The Optimal default setting for this option is Suspend and the Fail-Safe default setting is Disabled.**

**Hard Disk Timeout (Minutes)**

This option specifies the length of a period of hard disk drive inactivity. When this length of time expires, the computer enters power-conserving state specified in the Hard Disk Power Down Mode option. The settings are **Disabled** and *1 Min through 15 Min in 1 minute intervals*.

**Power Saving Type**

The settings for this option are **Sleep**, *Stop Clock* or *Deep Sleep*.

**Standby/Suspend Timer Unit**

This allows you to set the standby timeout and suspend timeout timer unit. The settings are *32 secs*, *4 msecs*, **4 min** or *4 secs*.

**Standby Timeout**

This option specifies the length of a period of system inactivity while in full power on state. When this length of time expires, the computer enters standby power state. The settings are **Disabled** and *4 Min through 508 Min in 4 minute intervals*.

**Suspend Timeout (Minutes)**

This option specifies the length of a period of system inactivity while in standby state. When this length of time expires, the computer enters suspend power state. The settings are **Disabled** and *4 Min through 508 Min in 4 minute intervals*.

**Slow Clock Ratio**

The value of the slow clock ratio indicates the percentage of time the STPCLK# signal is asserted while in the thermal throttle mode. The settings are *Disabled*, *0-12.5%*, *12.5-25%*, *25-37.5%*, *37.5-50%*, **50-62.5%**, *62.5-75%*, or *75-87.5%*.

**Display Activity**

This option specifies if AMIBIOS is to monitor display activity for power conservation purposes. When this option is set to *Monitor* and there is no display activity for the length of time specified in the Standby Timeout (Minute) option, the computer enters a power savings state. The settings are *Monitor* or **Ignore**.

**Device 6 (Serial port 1)**

**Device 7 (Serial port 2)**

**Device 8 (Parallel port)**

**Device 5 (Floppy disk)**

**Device 0 (Primary Master IDE)**

**Device 1 (Primary Slave IDE)**

**Device 2 (Secondary Master IDE)**

**Device 3 (Secondary Slave IDE)**

When set to *Monitor*, these options enable event monitoring on the specified hardware interrupt request line. If set to *Monitor* and the computer is in a power saving state, AMIBIOS watches for activity on the specifies IRQ line. The computer enters the Full On state if any activity occurs. AMIBIOS reloads the Standby and Suspend timeout timers if activity occurs on the specified IRQ line. **Note: The Optimal default setting for each option is Ignore with the exception of Devices 0 (Primary Master IDE) and 6 (Serial Port 1) which should be set to Monitor. The Fail-Safe default for each option is Monitor.**

**LAN Wake-Up**

**RTC Wake-Up**

Options for LAN Wake-Up and RTC (Real Time Clock) Wake-Up are **Disabled** or **Enabled**. When RTC Wake-Up is enabled, the **Hour** and **Minute** settings can be set to the desired wake-up time relative to the current real time clock.

## **PCI/PnP Setup**

**Plug and Play-Aware OS**

The settings for this option are **No** or **Yes**. Set this option to **Yes** if the operating system in the computer is aware of and follows the Plug and Play specification. AMIBIOS only detects and enables PnP ISA adapter cards that are required for system boot. Currently, only Windows 95 is PnP-Aware. Set this option to **No** if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. You must set this option correctly. Otherwise, PnP-aware adapter cards installed in the computer will not be configured properly.

**PCI Latency Timer (PCI Clocks)**

This option specifies the latency timings in PCI clocks for all PCI devices. The settings are 32, **64**, 96, 128, 160, 192, 224, or 248.

**PCI VGA Palette Snoop**

The settings for this option are **Disabled** or **Enabled**. When set to **Enabled**, multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit (0 is disabled). For example: if there are two VGA devices in the computer (one PCI and one ISA) and this option is disabled, data read and written by the CPU is only directed to the PCI VGA device's palette registers. If enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA palette registers. This will permit the palette registers of both devices to be identical. This option must be set to **Enabled** if any ISA adapter card installed in the system requires VGA palette snooping.

**PCI IDE Busmaster**

The settings for this option are **Disabled** or **Enabled**. Set to **Enabled** to specify the IDE Controller on the PCI bus has bus mastering capabilities. Under Windows 95, you should set this option to **Disabled** and install the Bus Mastering driver.

**Offboard PCI IDE Card**

This option specifies if an offboard PCI IDE controller adapter card is installed in the computer. The PCI expansion slot on the motherboard where the offboard PCI IDE controller is installed must be specified. If an offboard PCI IDE controller is used, the onboard IDE controller is automatically disabled. The settings are **Auto** (AMIBIOS automatically determines where the offboard PCI IDE controller adapter card is installed), *Slot 1*, *Slot 2*, *Slot 3*, *Slot 4*, *Slot 5* or *Slot 6*.

This option forces IRQ14 and IRQ15 to a PCI slot on the PCI local bus. This is necessary to support non-compliant ISA IDE controller adapter cards. If an offboard PCI IDE controller adapter card is installed in the computer, you must also set the Offboard PCI IDE Primary IRQ and Offboard PCI IDE Secondary IRQ options.

**Offboard PCI IDE Primary IRQ****Offboard PCI IDE Secondary IRQ**

These options specify the PCI interrupt used by the primary (or secondary) IDE channel on the offboard PCI IDE controller. The settings are **Disabled**, **Hardwired**, **INTA**, **INTB**, **INTC**, or **INTD**.

**PCI Slot1 IRQ Priority****PCI Slot2 IRQ Priority****PCI Slot3 IRQ Priority****PCI Slot4 IRQ Priority**

These options specify the IRQ priority for PCI devices installed in the PCI expansion slots. The settings are **Auto**, (IRQ) 3, 4, 5, 7, 9, 10, 11, 12, 14, or 15, in priority order.

**DMA Channel 0****DMA Channel 1****DMA Channel 3****DMA Channel 5****DMA Channel 6****DMA Channel 7**

These DMA channels control the data transfers between the I/O devices and the system memory. The chipset allows the BIOS to choose which channels to do the job. The settings are **PnP** or **ISA/EISA**.

**IRQ3****IRQ4****IRQ5****IRQ7****IRQ9****IRQ10****IRQ11****IRQ12****IRQ14****IRQ15**

These options specify which bus the specified IRQ line is used on and allow you to reserve IRQs for legacy ISA adapter cards. If more IRQs must be removed from the pool, the end user can use these options to reserve the IRQ by assigning an **ISA/EISA** setting to it. Onboard I/O is configured by AMIBIOS. All IRQs used by onboard I/O are configured as **PCI/PnP**.

IRQ14 and 15 will not be available if the onboard PCI IDE is enabled. If all IRQs are set to **ISA/EISA** and IRQ14 and 15 are allocated to the onboard PCI IDE, IRQ 9 will still be available for PCI and PnP devices. This is because at least one IRQ must be available for PCI and PnP devices. The settings are **PCI/PnP** or **ISA/EISA**.

***Reserved Memory Size***

This option specifies the size of the memory area reserved for legacy ISA adapter cards. The settings are ***Disabled***, ***16K***, ***32K*** or ***64K***.

***Reserved Memory Address***

This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards. The settings are ***C8000***, ***CC000***, ***D0000***, ***D4000***, ***D8000*** or ***DC000***.

***PCI Device Search Order***

The settings are ***First-Last*** or ***Last-First***. This option selects the search priority during system startup of the PCI card slots; starting from PCI 1 thru PCI 4 (First-Last) or PCI 4 thru PCI 1 (Last-First).

***Default Primary Video***

This feature supports multiple displays, and selects the default video device based on card type. The settings are ***AGP*** or ***PCI***.

## **Peripheral Setup**

***Remote Power On***

Microsoft's Memphis OS supports this feature which can wake-up the system from SoftOff state through devices (such as an external modem) that are connected to COM1 or COM2. The settings are ***Disabled*** or ***Enabled***.

***CPU Current Temperature***

The current CPU temperature is displayed in this option. ***Note: This option shows both CPU1 and CPU2 , but CPU2 is grayed out with only one Celeron processor.***

***CPU Overheat Warning***

The settings for this option are ***Enabled*** or ***Disabled***. When set to ***Enabled*** this option allows the user to set an overheat warning temperature.

***CPU Overheat Warning Temperature***

This option is *grayed out* for the Celeron processor, but is available for the Pentium II processor.

***H/W Monitor In0 (CPU 1)***

***H/W Monitor In1 (CPU 2 - grayed out for Celeron processor)***

***H/W Monitor In2 (+3.3V)***

***H/W Monitor In3 (+5V)***

***H/W Monitor In4 (+12V)***

***H/W Monitor In5 (-12V)***

***H/W Monitor In6 (-5V)***

***CPU1 Fan***

***CPU2 Fan (grayed out for Celeron processor)***

***Thermal Control Fan (grayed out for Celeron processor)***

The above features are for PC Health Monitoring. The motherboards with W83781D have seven on-board voltage monitors for the CPU core, CPU I/O, +3.3V, +5V, -5V, +12V, and -12V, and three fan status monitors.

### ***Power Loss Control***

This option determines how power is restored in the event of AC power loss. Settings are: ***Always OFF***, ***Always ON***, or ***Previous***. Always OFF provides no automatic power loss control, and power is controlled by the chassis POWER switch. Always ON will automatically power-on the system whenever source power is applied to the system (the power cord is plugged in). The Previous setting remembers the previous power state (ON or OFF), and restores that power state upon the return of source power.

### ***Keyboard Wake-up Function***

This option allows the system to 'wake-up' from standby or sleep mode by pressing any key on the keyboard. Settings are ***Disabled*** or ***Enabled***.

***Note: The JPWAKE jumper on the system board must be set to 2-3 before the Enabled setting will work.***

### ***On-Board FDC***

This option enables the FDC (Floppy Drive Controller) on the motherboard. The settings are ***Auto*** (AMIBIOS automatically determines if the floppy controller should be enabled), ***Disabled***, or ***Enabled***.

### ***On-Board Serial Port A***

This option specifies the base I/O port address of serial port 1. The settings are ***Auto*** (AMIBIOS automatically determines the correct base I/O port address), ***Disabled***, ***3F8h/COM1***, ***2F8h/COM2***, ***3E8h/COM3*** or ***2E8h/COM4***.

**On-Board Serial Port B**

This option specifies the base I/O port address of serial port 2. The settings are *Auto* (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, *3F8h/COM1*, ***2F8h/COM2***, *3E8h/COM3* or *2E8h/COM4*.

**IR Port Support**

This option enables the infrared port feature on the system board. Settings are: ***Disabled*** or *Enabled*. If Enabled, the following settings can be made:

**IR Mode Select**

Settings are: *Yes*, *ASK IR*, *High*, or *Off*.

**IR Base Address Select**

Settings are: *Slow*, *Fast*, *Absent*, or *Present*.

**IR IRQ Select**

Settings are: 3, 4, 9, 10, or 11.

**IR DMA Select**

Settings are: *Disabled*, 0, 1, or 3.

**On-Board Parallel Port**

This option specifies the base I/O port address of the parallel port on the motherboard. The settings are *Auto* (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, ***378***, *278* or *3BC*.

**Parallel Port Mode**

This option specifies the parallel port mode. The settings are *Normal*, *Bi-Dir*, *EPP* or *ECP*. When set to *Normal*, the normal parallel port mode is used. Use *Bi-Dir* to support bidirectional transfers. Use *EPP* (Enhanced Parallel Port) to provide asymmetric bidirectional data transfer driven by the host device. Use *ECP* (Extended Capabilities Port) to achieve data transfer rates of up to 2.5 Mbps. ECP uses the DMA protocol and provides symmetric bidirectional communication. **Note: The Optimal default setting for this option is ECP and the Fail-Safe setting is Normal.**

**EPP Version**

The settings are 1.7 or 1.9.

**Parallel Port IRQ**

This option specifies the IRQ to be used by the parallel port. The settings are ***Auto***, 5 or 7.

### ***Parallel Port DMA Channel***

This option is only available if the setting of the parallel port mode option is *ECP*. The settings are 0, 1, 2, 3, 5, 6 or 7.

### ***On-Board IDE***

This option specifies the onboard IDE controller channels to be used. The settings are *Disabled*, *Primary*, *Secondary* or ***Both***.

## **5-2 Security Setup**

### **Supervisor/User**

The system can be configured so that all users must enter a password every time the system boots or when the WINBIOS setup is executed. You can set either a Supervisor password or a User password. If you do not want to use a password, just press <Enter> when the password prompt appears.

The password check option is enabled in the Advanced Setup by choosing either *Always* or *Setup*. The password is stored in CMOS RAM. You can enter a password by typing the password on the keyboard, selecting each letter via the mouse, or selecting each letter via the pen stylus. Pen access must be customized for each specific hardware platform.

When you select Supervisor or User, AMIBIOS prompts for a password. You must set the Supervisor password before you can set the User password. Enter a 1-6 character password. The password does not appear on the screen when typed. Retype the new password as prompted and press <Enter>. Make sure you write it down. If you forget it, you must drain CMOS RAM and reconfigure.



## 5-3 Utility Setup

### Anti-Virus

When this icon is selected, AMIBIOS issues a warning when any program (or virus) issues a disk format command or attempts to write to the boot sector of the hard disk drive. The settings are *Enabled* or *Disabled*.

### Language

**Note:** *The Optimal and Fail-Safe default settings for this option are English.*

## 5-4 Default Setting

Every option in WinBIOS Setup contains two default settings: a Fail-Safe default, and an Optimal default.

### Optimal Default

The Optimal default settings provide optimum performance settings for all devices and system features.

### Fail-Safe Default

The Fail-Safe default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

## Notes

## Appendix A

# BIOS Error Beep Codes & Messages

During the POST (Power-On Self-Test) routines, which are performed each time the system is powered on, errors may occur.

**Non-fatal errors** are those which, in most cases, allow the system to continue the boot-up process. The error messages normally appear on the screen.

**Fatal errors** are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list, on the following page, correspond to the number of beeps for the corresponding error. All errors listed, with the exception of #8, are fatal errors.

Beeps	Error message	Description
1	Refresh Failure	The memory refresh circuitry on the motherboard is faulty.
2	Parity Error	A parity error was detected in the base memory (the first 64 KB block) of the system.
3	Base 64 KB Memory Failure	A memory failure occurred within the first 64 KB of memory.
4	Timer Not Operational	A memory failure was detected in the first 64 KB of memory, or Timer 1 is not functioning.
5	Processor Error	The CPU on the system board generated an error.
6	8042 - Gate A20 Failure	The keyboard controller (8042) contains the Gate A20 switch which allows the CPU to operate in virtual mode. This error means that the BIOS cannot switch the CPU into protected mode.
7	Processor Exception Interrupt Error	The CPU on the motherboard generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. <b>Please Note:</b> This is not a fatal error.
9	ROM Checksum Error	The ROM checksum value does not match the value encoded in the BIOS.
10	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS memory has failed.

Refer to the table on page A-3 for solutions to the error beep codes.

<b>If it beeps...</b>	<b>then ...</b>
1, 2, 3 times	reseat the DIMM memory. If the system still beeps, replace the memory.
6 times	reseat the keyboard controller chip. If it still beeps, replace the keyboard controller. If it still beeps, try a different keyboard, or replace the keyboard fuse, if the keyboard has one.
8 times	there is a memory error on the video adapter. Replace the video adapter, or the RAM on the video adapter.
9 times	the BIOS ROM chip is bad. The system probably needs a new BIOS ROM chip.
4, 5, 7, or 10 times	the motherboard must be replaced.

Error Message	Information
8042 Gate -- A20 Error	Gate A20 on the keyboard controller (8042) is not working. Replace the 8042.
Address Line Short!	Error in the address decoding circuitry on the motherboard.
C: Drive Error	Hard disk drive C: does not respond. Run the Hard Disk Utility to correct this problem. Also, check the C: hard disk type in Standard Setup to make sure that the hard disk type is correct.
C: Drive Failure	Hard disk drive C: does not respond. Replace the hard disk drive.
Cache Memory Bad	Cache memory is defective. Replace it. Do Not Enable Cache!
CH-2 Timer Error	Most ISA computers include two times. There is an error in time 2.
CMOS Battery State Low	CMOS RAM is powered by a battery. The battery power is low. Replace the battery.
CMOS Checksum Failure	After CMOS RAM values are saved, a checksum value is generated for error checking. The previous value is different from the current value. Run WINBIOS Setup or AMIBIOS Setup.
CMOS System Option Not Set	The values stored in CMOS RAM are either corrupt or nonexistent. Run WINBIOS Setup or AMIBIOS Setup.
CMOS Display Type Mismatch	The video type in CMOS RAM does not match the type detected by the BIOS. Run WINBIOS Setup or AMIBIOS Setup.
CMOS Memory Size Mismatch	The amount of memory on the motherboard is different than the amount in CMOS RAM. Run WINBIOS Setup or AMIBIOS Setup.

<b>Error Message</b>	<b>Information</b>
CMOS Time and Date Not Set	Run Standard Setup to set the date and time in CMOS RAM.
D: Drive Error	Hard disk drive D: does not respond. Run the Hard Disk Utility. Also check the D: hard disk type in Standard Setup to make sure that the hard disk drive type is correct.
D: Drive Failure	Hard disk drive D: does not respond. Replace the hard disk.
Diskette Boot Failure	The boot disk in floppy drive A: is corrupt. It cannot be used to boot the computer. Use another boot disk and follow the screen instructions.
Display Switch Not Proper	Some computers require a video switch on the motherboard be set to either color or monochrome. Turn the computer off, set the switch, then power on.
DMA Error	Error in the DMA controller.
DMA #1 Error	Error in the first DMA channel.
DMA #2 Error	Error in the second DMA channel.
FDD Controller Failure	The BIOS cannot communicate with the floppy disk drive controller. Check all appropriate connections after the computer is powered down.
HDD Controller Failure	The BIOS cannot communicate with the hard disk drive controller. Check all appropriate connections after the computer is powered down.
INTR #1 Error	Interrupt channel 1 failed POST.
INTR #2 Error	Interrupt channel 2 failed POST.

Error Message	Information
Invalid Boot Diskette	The BIOS can read the disk in floppy drive A:, but cannot boot the computer. Use another boot disk.
Keyboard Is Locked... Unlock It	The keyboard lock on the computer is engaged. The computer must be unlocked to continue.
Keyboard Error	There is a timing problem with the keyboard. Set the <i>Keyboard</i> options in Standard Setup to <i>Not Installed</i> to skip the keyboard post routines.
KB/Interface Error	There is an error in the keyboard connector.
No ROM BASIC	Cannot find a bootable sector on either disk drive A: or hard disk drive C:. The BIOS calls INT 18h which generates this message. Use a bootable disk.
Off Board Parity Error	Parity error in memory installed in an expansion slot. The format is: OFF BOARD PARITY ERROR ADDR (HEX) = (XXXX) XXXX is the hex address where the error occurred. Run AMIDiag to find and correct memory problems.
On Board Parity Error	Parity error in motherboard memory. The format is: ON BOARD PARITY ERROR ADDR (HEX) = (XXXX) XXXX is the hex address where the error occurred. Run AMIDiag to find and correct memory problems.
Parity Error????	Parity error in system memory at an unknown address. Run AMIDiag to find and correct memory problems.



## Appendix B

### AMI BIOS POST Diagnostic Error Messages

This section describes the power-on self-tests (POST) port 80 codes for the AMI BIOS.

#### Check

<u>Point</u>	<u>Description</u>
00	Code copying to specific areas is done. Passing control to INT 19h boot loader next.
03	NMI is Disabled. Next, checking for a soft reset or a power-on condition.
05	The BIOS stack has been built. Next, disabling cache memory.
06	Uncompressing the post code unit next.
07	Next, initializing the CPU init and the CPU data area.
08	The CMOS checksum calculation is done next.
0B	Next, performing any required initialization before keyboard BAT command is issued.
0C	The keyboard controller I/B is free. Next, issuing the BAT command to the keyboard controller.
0E	The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
0F	The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next.

<b>Check Point</b>	<b>Description</b>
10	The keyboard controller command byte is written. Next, issuing the pin 23 and 24 blocking and unblocking commands.
11	Next, checking if the <End or <Ins> keys were pressed during power on. Initializing CMOS RAM if the Initialize CMOS RAM in every boot AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.
12	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14	The 8254 timer test will begin next.
19	The 8254 timer test is over. Starting the memory refresh test next.
1A	The memory refresh test line is toggling. Checking the 15 second on/off time next.
23	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24	The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
25	Interrupt vector initialization is done. Clearing the password if the POST DIAG Switch is on.
27	Any initialization before setting video mode will be done next.

<b><u>Check Point</u></b>	<b><u>Description</u></b>
28	Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
2A	Bus initialization system, static, output devices will be done next, if present.
2B	Passing control to the video ROM to perform any required configuration before the video ROM test.
2C	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.
2D	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
2E	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2F	The EGA/VGA controller was not found. The display memory read/write test is about to begin.
30	The display memory read/write test passed. Look for retrace checking next.
31	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next.
32	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34	Video display checking is over. Setting the display mode next.
37	The display mode is set. Displaying the power on message next.

<b><u>Check Point</u></b>	<b><u>Description</u></b>
38	Initializing the bus input, IPL, and general devices next, if present.
39	Displaying bus initialization error messages.
3A	The new cursor position has been read and saved. Displaying the Hit <DEL> message next.
40	Preparing the descriptor tables next.
42	The descriptor tables are prepared. Entering protected mode for the memory test next.
43	Entered protected mode. Enabling interrupts for diagnostics mode next.
44	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46	The memory wraparound test has completed. The memory size calculation has been completed. Writing patterns to test memory next.
47	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next.
48	Patterns written in base memory. Determining the amount of memory below 1 MB next.
49	The amount of memory below 1 MB has been found and verified. Determining the amount of memory above 1 MB memory next.
4B	The amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.

<b><u>Check Point</u></b>	<b><u>Description</u></b>
4C	The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next.
4D	The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next.
4E	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.
4F	The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next.
50	The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.
51	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB next.
52	The memory above 1 MB has been tested and initialized. Saving the memory size information next.
53	The memory size information and the CPU registers are saved. Entering real mode next.
54	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58	The memory size was adjusted for relocation and shadowing. Clearing the Hit <DEL> message next.
59	The Hit <DEL> message is cleared. The <WAIT> message is displayed. Starting the DMA and interrupt controller test next.

<b>Check Point</b>	<b>Description</b>
60	The DMA page register test passed. Performing the DMA Controller 1 base register test next.
62	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next.
65	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
66	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next.
7F	Extended NMI source enabling is in progress.
80	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83	The command byte was written and global data initialization has been completed. Checking for a locked key next.
84	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85	The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.
86	The password was checked. Performing any required programming before WINBIOS Setup next.

<b>Check Point</b>	<b>Description</b>
87	The programming before WINBIOS Setup has been completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.
88	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next.
89	The programming after WINBIOS Setup has been completed. Displaying the power-on screen message next.
8B	The first screen message has been displayed. The <WAIT...> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
8C	Programming the WINBIOS Setup options next.
8D	The WINBIOS Setup options are programmed. Resetting the hard disk controller next.
8F	The hard disk controller has been reset. Configuring the floppy drive controller next.
91	The floppy drive controller has been configured. Configuring the hard disk drive controller next.
95	Initializing the bus option ROMs from C800 next.
96	Initializing before passing control to the adaptor ROM at C800.
97	Initialization before the C800 adaptor ROM gains control has been completed. The adaptor ROM check is next.
98	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.

<b>Check Point</b>	<b>Description</b>
99	Any initialization required after the option ROM test has been completed. Configuring the timer data area and printer base address next.
9A	Set the timer and printer base addresses. Setting the RS-232 base address next.
9B	Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.
9C	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9D	Coprocessor initialized. Performing any required initialization after the Coprocessor test next.
9E	Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2	Displaying any soft errors next.
A3	The soft error display has completed. Setting the keyboard typematic rate next.
A4	The keyboard typematic rate is set. Programming the memory wait states next.
A5	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.



<b><u>Check Point</u></b>	<b><u>Description</u></b>
A9	Returned from adaptor ROM at E000h control. Next, performing any initialization required after the E000 option ROM had control.
AA	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
AB	Building the multiprocessor table, if necessary. POST next.
B0	The system configuration is displayed.
AC	Uncompressing the DMI data and initializing DMI.
B1	Copying any code to specific areas.
D0h	The NMI is disabled. Power on delay is starting. Next, the initialization code checksum will be verified.
D1h	Initializing the DMA controller. Performing the keyboard controller BAT test. Starting memory refresh, and entering 4 GB flat mode next.
D3h	Starting memory sizing next.
D4h	Returning to real mode. Executing any OEM patches and setting the stack next.
D5h	Passing control to the uncompressed code in shadow RAM at E000:0000h. The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Control is in segment 0. Next, checking if <Ctrl><Home>was pressed and verifying the system BIOS checksum.  If either <Ctrl><Home>was pressed or the system BIOS checksum is bad, next the system will go to checkpoint code E0h.  Otherwise, going to checkpoint code D7h.

## Notes